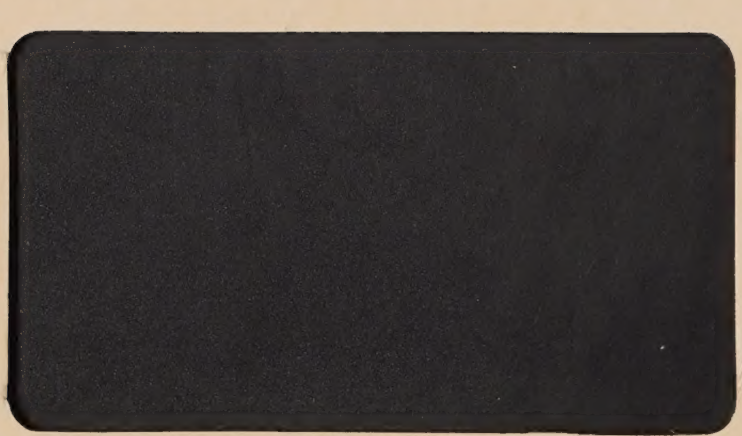
INSTRUCTION MANUAL

1159

Reciprocatic Counter

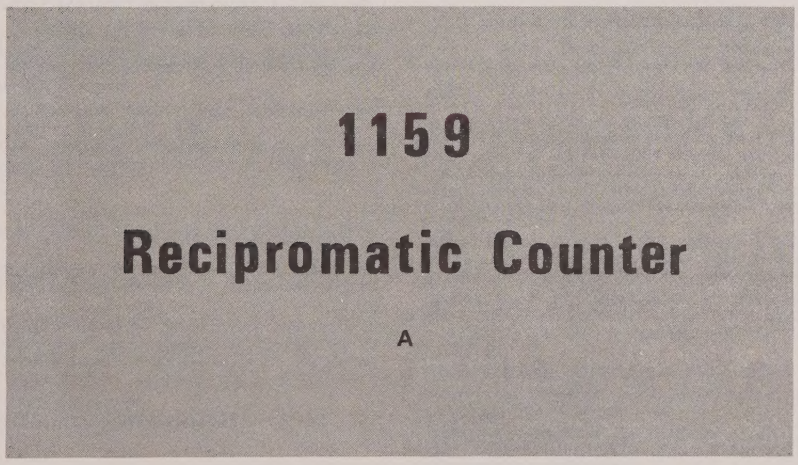
A

GENERAL RADIO



WARRANTY

We warrant that each new instrument manufactured and sold by us is free from defects in material and workmanship and that, properly used, it will perform in full accordance with applicable specifications for a period of two years after original shipment. Any instrument or component that is found within the two-year period not to meet these standards after examination by our factory, District Office, or authorized repair agency personnel, will be repaired or, at our option, replaced without charge, except for tubes or batteries that have given normal service.



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GENERAL RADIO COMPANY
West Concord, Massachusetts U.S.A. 01781
Form 1159-0100-A
December, 1968
ID-B100

Condensed Operating Instructions

POWER

The 1159 can be used with either 115-V ac or 230-V ac line voltage. Place S502 (rear-panel line switch) to the proper position before connecting the instrument to a power source.

MANUAL

Front Panel

a. Connect signal source to INPUT.
b. Place POWER ON/OFF switch to ON.
c. Place MEAS RATE switch to FAST for signals above 8-Hz; SLOW for signals below 6-Hz; or AUTO for automatic clock-rate switching.
d. Place TRIG LEVEL control to mid-range. (Adjustment required for stability only on small pulse signals.)
e. Select the appropriate band for signal being measured with INPUT BAND switch.
f. Set DISPLAY TIME control for desired display period.
g. The RESET button is used to initiate a count cycle when the DISPLAY TIME control is in the HOLD position.

Rear Panel

a. Place PRESCALER FACTOR switch to:
   X1 for normal operation
   X10 for use with 10:1 scaler
   X100 for use with 100:1 scaler
b. Place EXT STD FREQ switch to either position if an external reference phase lock signal is used (1 MHz or 100 kHz).

PROGRAMMED

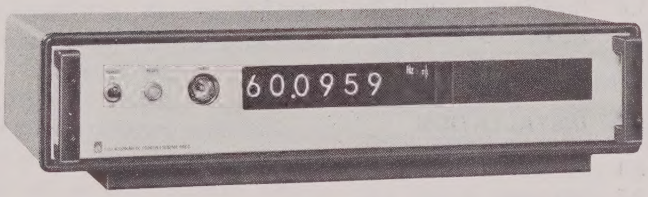
Front Panel

a. Place SLOPE switch to $\overset{+}{R}$
b. Place MEAS RATE switch to AUTO R.
c. Place TRIG LEVEL control full cw to REMOTE.
d. Place INPUT BAND switch to 10-MHz-R.
e. Place DISPLAY TIME control full cw to HOLD-R.

Rear Panel

a. Place PRESCALER FACTOR switch to X1.
b. Place EXT STD FREQ switch to 1-MHz.
c. Connect the programming source to SO905.

Specifications



specifications

Frequency-Measurement Range: 0.6 Hz to 20 MHz. In the fast mode, 6 Hz to 20 MHz; in the slow mode, 0.6 Hz to 9.99999 MHz. Extend range to 100 or 500 MHz without loss of accuracy with GR 1156 (10:1) or 1157 (100:1) Scaler.

Frequency-Measurement Accuracy: ±0.5 in least significant digit ±1 x 10^{-6} ± clock accuracy ± noise (see note).

Measurement Rate: Sum of adjustable display time, 0.02 to 10 s and ∞, and measurement time of about 100 ms in fast mode or 1 s in slow mode.

INPUT

Sensitivity: 20 mV rms at 20 MHz; 10 mV rms from 1 Hz to 10 MHz.

Bandwidth: Ac-coupled input, −3 dB at approx 1 Hz. Bandwidth switch sets −3 dB points at approx 10 or 1 MHz, 100, 10, or 1 kHz.

Impedance: 1 MΩ//27 pF for up to 5-V pk-pk input; 0.67 MΩ//30 pF for up to 200 V pk-pk. Input capacitance can be reduced by disconnecting either unused front- or rear-panel input connector. Front only, 20 pF; rear only, 17 pF.

Trigger Threshold: ±20 mV, adjustable.

Slope: Positive- or negative-going, switch-selected.

CLOCK

Internal: 10-MHz, third-overtone quartz-crystal oscillator in proportional-controlled oven.

Temperature Effects: $<1 \times 10^{-6}$ from 0 to 50°C ambient.

Warmup: Within 1 x 10^{-6} after 10 minutes at 25°C ambient.

Stability: Better than 3×10^{-9} per day after 1 month of operation; better than 1×10^{-6} per year.

External Control: Internal clock oscillator can be phase-locked to external 100-kHz or 1-MHz signal of at least 1 V rms.

GENERAL

Programmability: All control functions can be programmed by contact closures to ground (2- to 4-mA sink current required) except display time, which requires an external resistance of 0 to 100 kΩ, and trigger level, which requires 0 to ±5 V dc for ±20-mV control.

Data Output: 1-2-4-8 BCD-DTL output for 6 digits of data, decimal point, and measurement units. Data zero is 0.5 V max (12-mA current sinking capability); data one is approx 5 V behind 6 kΩ.

Display: Six neon readout tubes, automatically positioned decimal point, and measurement units. Dimensions can be multiplied by 1, 10, or 100 with rear-panel switch for use with 10:1 or 100:1 prescaler.

Power Required: 100 to 125 or 200 to 250 V, 50 to 400 Hz, 60 W.

Accessories Supplied: Power cord, spare fuses, mounting hardware with rack models.

Accessories Available: GR 1156 (10:1) and 1157 (100:1) Scalers, 1137 Data Printer, 1136 Digital-to-Analog Converter, other GR data-handling equipment.

Mounting: Bench model (in metal cabinet) or rack model.

Dimensions (width x height x depth): Bench, 19¾ x 4⅞ x 15 in. (500 x 125 x 385 mm); rack, 19 x 3½ x 13¼ in. (485 x 89 x 340 mm).

Net Weight: Bench, 26 lb (12 kg); rack, 19 lb (9 kg).

Shipping Weight: Bench, 35 lb (16 kg); rack, 28 lb (13 kg).

Note — Noise affects precision of frequency measurement. For additive noise on signal measured, the error in measurement will be $\varepsilon = \frac{N}{\pi S\sqrt{n}}$ where N is the noise level and S the signal level in the same units; n is the number of periods averaged. Internally produced noise in the counter will determine the limiting error level. For the 1159, this internal noise is approx 50 μV rms.

Catalog Number	Description
	1159 Reciprocmatic Counter
1159-9700	Bench Model
1159-9701	Rack Model

Contents

Section 1 — INTRODUCTION

1.1 Purpose 1-1
1.2 General Description 1-1
1.3 Front Panel Controls and Connectors 1-2
1.4 Rear Panel Controls and Connectors 1-3
1.5 Accessories Supplied 1-3
1.6 Patch Cords and Adaptors 1-6

Section 2 — INSTALLATION

2.1 Power Connections 2-1
2.2 Mounting 2-1
2.3 Interconnections 2-3

Section 3 — OPERATION

3.1 General 3-1
3.2 Preliminary Checks 3-1
3.3 Operational Check 3-1
3.4 Manual Operation 3-1
3.5 Programmed Operation 3-2

Section 4 — THEORY

4.1 Introduction 4-1
4.2 Special Logic Circuits 4-1
4.3 Detailed Logic Description 4-4
4.4 Circuit Descriptions 4-7

Section 5 — SERVICE AND MAINTENANCE

5.1 Service 5-1
5.2 Instrument Return 5-1
5.3 Minimum Performance Standards 5-1
5.4 Component Accessibility 5-4
5.5 Maintenance 5-4
5.6 Trouble Analysis 5-5
5.7 Calibration 5-9

Section 6 — DIAGRAMS AND PARTS LISTS 6-1

Introduction—Section 1

1.1 PURPOSE.

The 1159 Reciprocatic Counter uses a built-in computer to combine the resolution and speed of a period measurement with the convenience of direct frequency readout. The computer also selects the measurement range automatically, so that the result is always displayed as a 6-digit number with the measurement units correctly labeled and the decimal point correctly positioned.

The 1159 has a minimum of operator panel controls with full external programming capabilities. The BCD data output can be used to plot, record, or compute from the measurement results. The GR 1137 Data Printer will produce a permanent printed record of up to 12 digits, enough capacity for counter data as well as such corollary information as channel numbers from an input scanner. The GR 1136 Digital-to-Analog Converter will provide frequency data to a recorder from the 1159 counter in suitable analog form to plot, for example, frequency as a function of temperature. The automatic features of the counter allow scanning of as many as 100 signal lines when used with the GR 1770 scanner.

The time base of the 1159 is controlled by a stable 10-MHz crystal oscillator in a proportional-controlled oven. Its rapid warmup and high stability characteristics ensure that the full accuracy of the 1159 is available promptly and will be maintained for long periods between recalibrations. The oscillator can also be phase-locked to an external 100-kHz or 1-MHz reference.

1.2 GENERAL DESCRIPTION.

1.2.1 Electrical Description.

The 1159 Reciprocatic Counter is an automatic frequency-measuring instrument. It contains a computer that selects the proper measurement range and correctly positions the decimal point. All readouts are in 6-digit numbers. The few necessary controls have a full range in both manual and programmed operation. Output data is available as BCD for driving a printer or other data handling equipment. The time base is controlled by a 10-MHz third-overtone crystal oscillator in a proportional oven and is stable to 1×10^{-6} in 10 minutes, ready for use. Programming inputs are switch closures to ground, providing full control except for POWER ON, TRIGGER LEVEL and DISPLAY TIME.

1.2.2 Mechanical Description.

The 1159 has front panel controls for power, display reset, input signal, measuring rate, input band frequency and display time. Rear panel controls are for prescaler factor and external phase-lock frequency select. A front-panel jack receives the input signal and rear panel jacks receive the input and time base phase-lock signals. Six neon readout tubes display the frequency of the input signal with automatic correct placement of the decimal point.

The 1159 is available with either a bench or rack mounting cabinet. The bench cabinet is vented and features a tilt-base for convenience.

1.2.3 Applications.

The 1159 can be used in any frequency measurement where both speed and accuracy are needed. It is especially useful in accelerating the test and calibration of frequency sources such as oscillators, signal generators, and voltage-to-frequency converters, particularly at low frequencies. The automatic ranging capability can be used at frequencies up to 500 MHz by use of the GR 1156 or GR 1157 Scalers. When used in automatic frequency measuring systems, external programming requirements are minimal due to the few controls. A few of the areas of application for the 1159 counter are:

(1) underwater research — calibration of transducers, source signals,
(2) sound and vibration — predominantly low frequency,
(3) rotating devices — gyros, motors and
(4) voltage to frequency converters — calibration by measuring frequency output for a given voltage input.

The 1159 is virtually fully automatic when externally programmed, greatly facilitating tests in the preceding application areas. Figure 1-1 shows available frequency measuring combinations.

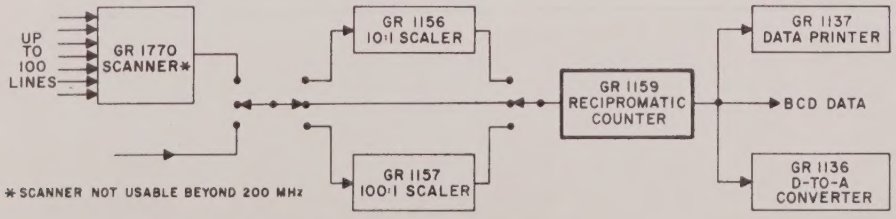


Figure 1-1. Available Combinations.

1.3 FRONT PANEL CONTROLS AND CONNECTORS.

Table 1-1
FRONT PANEL CONTROLS AND CONNECTORS

Fig. 1-2 Ref	Name	Description	Function
1	POWER ON-OFF	Toggle Switch	Connects line power to instrument.
2	RESET	Push Button	Resets indicators to zero. When HOLD display time is used starts new measurement.
3	INPUT	GR874® Connector	Receives input signal frequency.
4	- - -	Neon Display Indicators	Display the measured frequency of the input signal.
5	Hz, kHz, MHz	Display Indicator	Indicates measured units.
6	NO SIGNAL	Display Indicator	Indicates signal amplitude is too low to trigger instrument.
7	LOW FREQ	Display Indicator	Indicates signal frequency below the range of the instrument (6-Hz for FAST, 0.6-Hz for SLOW).
8	SLOPE ±	Toggle Switch	Selects positive or negative trigger slope.
9	AUTO MEASURING RATE FAST–SLOW	Toggle Switch	Controls the measurement time – FAST, 100-ms, SLOW, 1 sec.
10	TRIG LEVEL	Ganged 2-position Switch and Potentiometer	Used only for pulses to control triggering level.
11	INPUT BAND 1-kHz, 10-kHz 100-kHz, 1-MHz 10-MHz	5-position Wafer Switch	Inserts proper low-pass filter to attenuate HF noise.
12	DISPLAY TIME	Ganged 2-position switch and Potentiometer	Selects variable delay time from .02 to 10 seconds or infinity in the HOLD position.

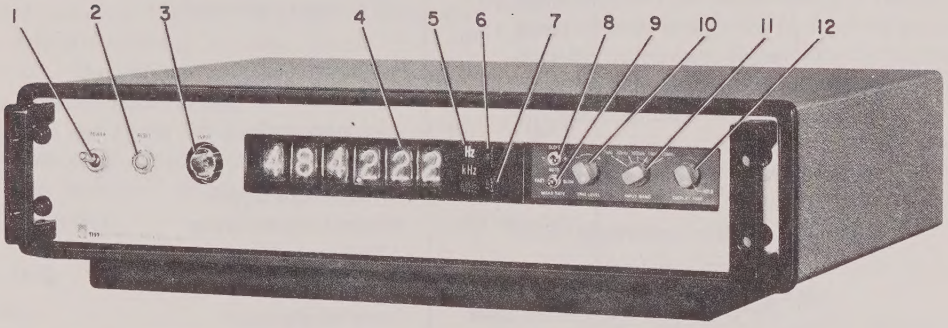


Figure 1-2. Front Panel.

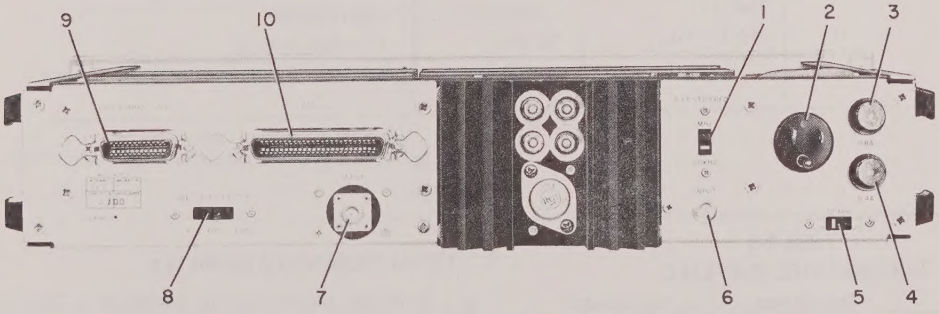


Figure 1-3. Rear Panel.

1.4 REAR PANEL CONTROLS AND CONNECTORS.

Table 1-2
REAR PANEL CONTROLS AND CONNECTORS

Fig 1-3 Ref	Name	Description	Function
1	EXT STD FREQ 1 MHz, 100 kHz	Slide switch 2-position	Selects external standard phase-lock frequency (1 MHz or 100 kHz).
2	- - - -	Polarized Power Plug	Line power connector.
3	F501	Fuse	Line power 110-V protection
4	F502	Fuse	Line power 220-V protection
5	- - - -	2-position slide switch	Switches line power connections for either 110-V ac or 220-V ac operation.
6	INPUT	BNC panel jack	External standard phase-lock frequency input. (1-MHz or 100-kHz).
7	INPUT	BNC panel jack.	Signal to be measured.
8	PRESCALER FACTOR X1, X10, X100	3-position slide switch	X1 for normal display X10 Multiplies readout by 10 X100 Multiplies readout by 100
9	PROGRAMMING INPUT	24-pin connector	Connects programming input signals
10	DATA OUT	50-pin connector	Provides access to data signals

Table 1-3
ACCESSORIES SUPPLIED

Quantity	Description	Part Number
1	Instruction Book	1159-0100
1	Fuse 0.4A (spare)	5330-0900
1	Fuse 0.8A (spare)	5330-1200
1	Power Cord, 7-foot 3-wire	4200-9622
4	Screws	7270-6310
1	Hardware Set*	4174-2000
4	Nuts*	5810-3300
4	Washers*	8040-2400
4	Washers*	8110-1300

*Supplied with rack mount version, P/N 4174-2000

1.5 ACCESSORIES SUPPLIED.

Supplied accessories are described in Table 1-3.

1.6 PATCH CORDS AND ADAPTORS.

A broad range of general-purpose patch cords is available to facilitate interconnection of the 1159 with other equipments. They are compatible with the GR874 and/or the BNC type coaxial connectors found on front and rear panels of the instrument.

In addition, an extensive selection of coaxial adaptors is available to permit use of the GR874 coaxial connectors on the front panel with most commercially available coaxial-connector systems.

Installation–Section 2

2.1 POWER CONNECTIONS.

Line power requirements for the 1159 are 100-125 V or 200-250 V, 50- to 400 Hz, 60 W. A line switch, S502, on the instrument rear panel (Figure 1-3) is used to switch the transformer primary windings to allow either 110-V or 220-V operation. The primary line power is properly fused by F501 and F502 at either voltage.

Connection to the power line is made by means of the 4200-9622 power cord, a 3-conductor cable with polarized connectors. See Section 6 for primary power and power-supply wiring diagrams.

2.2 MOUNTING.

2.2.1 General.

The 1159 is supplied in two models, bench mount and rack mount. Either model may be converted to the other by the installation of a simple conversion set.

2.2.2 Bench Mounting.

The bench-mount cabinet is made of formed and welded 1/8-inch aluminum finished in baked-on, medium gray wrinkly paint and has a tilt base. The instrument is retained in the case by four front panel screws accessible through holes in the carrying handles. A rear cover is attached to the instrument by two screws. To remove the instrument from the case, remove the four front panel screws and withdraw the instrument. Slide blocks on the instrument engage tracks in the case to guide insertion and withdrawal. To insert the instrument into the case, straddle the tracks with the rear guide blocks and push all the way into the case. Secure the four front panel screws.

2.2.3 Conversion to Rack Mounting.

The following procedure is used to convert a bench model to a rack mounted model.

a. Order rack-cabinet assembly (P/N 4174-3990) and a hardware set (P/N 4174-2000).

b. Disconnect any external cables, remove the front panel screws and withdraw the instrument from the case.

c. Remove the rear cover screws and rear cover from the bench cabinet. Secure the rear cover to the rack-cabinet with the rear cover screws.

d. Install the rack-cabinet in the relay rack and insert the instrument.

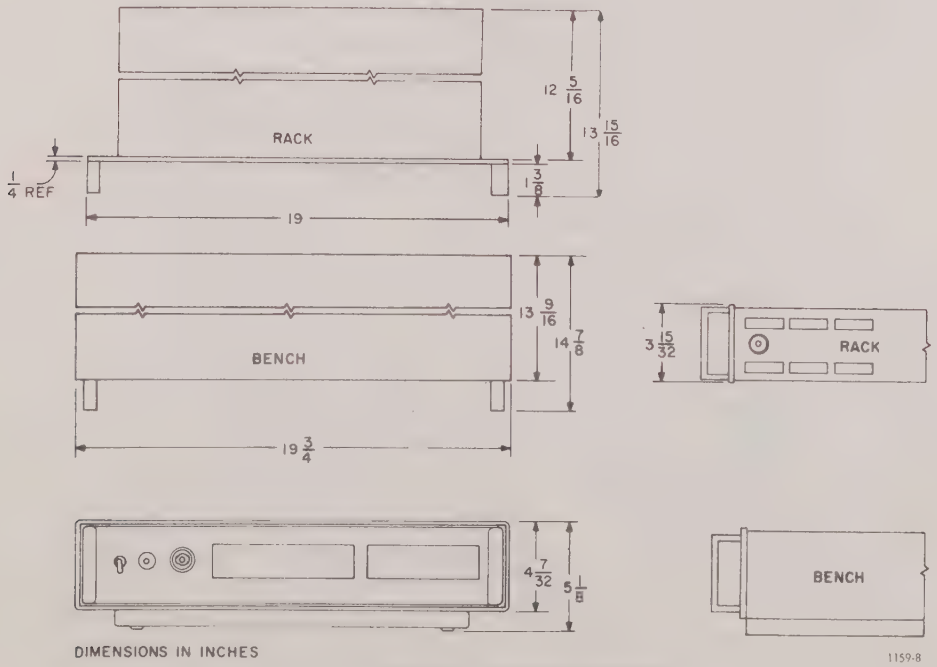


Figure 2-1. Mounting Dimensions.

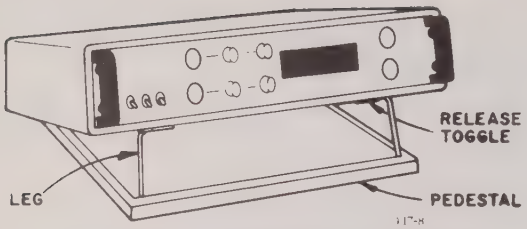


Figure 2-2. Tilt-Base Bench Mount Cabinet.

2.2.4 Rack Mounting.

A rack-mounting case with installation hardware is provided with the rack mount model. To install this model in a standard 19-inch relay-rack proceed as follows:

a. Remove the panel screws and withdraw the instrument until it stops. Lift the front and withdraw completely from the cabinet.

b. Insert the cabinet into the rack and secure it to the front of the rack with the four screws provided.

c. If the rack contains a rear support, remove the rear cover screws and rear cover from the case. Attach the brackets to the cabinet with the rear bracket screws and nuts provided. Use the set of slots that most nearly align the bracket with the rear support of the rack. Secure the brackets to the rack, each with two screws and nuts provided.

d. Push the track all the way into the case. Place the rear of the instrument into the cabinet, lifting it to straddle the tracks with the slide blocks. Push the instrument into the case until it stops. Lift the front, pull the instrument out so that the tracks follow and then push in so that the front slide blocks straddle the tracks. Slide the instrument all the way into the case and secure with four front panel screws.

2.2.5 Conversion to Bench Mounting.

a. Order a 4173-4000 bench cabinet assembly, two 4171-8601 tracks, two 4171-8802 rear brackets, and eight 7170-1308 screws.

b. Install the tracks to the front and rear channels inside the bench cabinet. Place the wide end of the track to the rear with the flat side against the channels. Secure each track with two screws.

c. Install the brackets to the rear channels inside the bench cabinet. Place the notch in the brackets around the tracks. Secure each bracket with two screws.

d. Disconnect any cables from the instrument, remove the front panel screws and withdraw the instrument from the rack cabinet.

e. Remove the rear cover screws and rear cover from the rack cabinet. Place the rear cover on the rear of the bench cabinet and secure it to the rear brackets with the rear cover screws.

f. Insert the instrument into the bench cabinet, straddling the tracks with the slide blocks. Secure the instrument with four front panel screws.

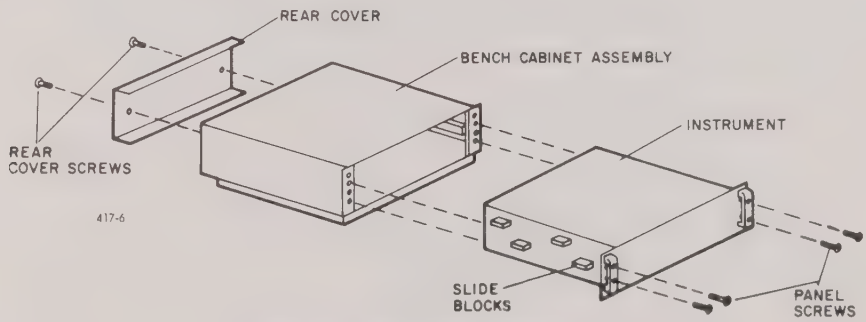


Figure 2-3. Bench Cabinet Assembly.

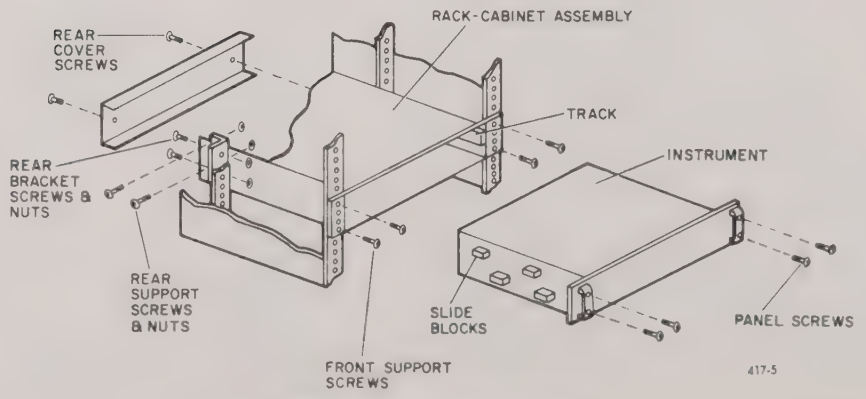


Figure 2-4. Relay-Rack Mounting.

2.3 INTERCONNECTIONS

2.3.1 Programming Input.

Programming Input Connector. The programming input signals connect to SO905, a 24-pin connector located on the instrument rear panel (see Figure 1-3) that mates with an Amphenol connector, P/N 57-30240. The wiring to the pins of SO905 from the instrument circuits is shown with associated signals in Figure 2-5.

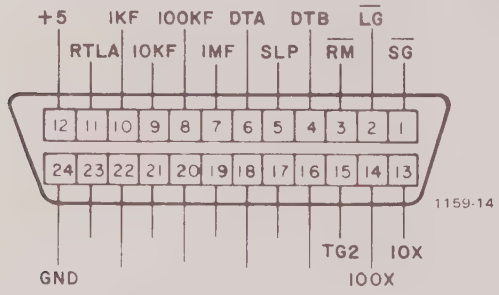


Figure 2-5. Programming Connector.

Programming Functions. The function of each of the programming inputs is given in Table 2-1.

2.3.2 Programming Characteristics.

Digital Programming Signal Characteristics. All control signals except Display Time and Trigger Level are digital with the following characteristics (voltages with respect to pin 24):

Absolute Maximum Ratings

Input forward current	−10 mA
Input reverse current	1 mA

Recommended Signal Levels for Proper Operation

	Minimum	Maximum
"Zero" level voltage	0 V	1.1 V
"One" level voltage	1.9 V	5.5 V
I_{In} for V_{In} = 0 V		−1.6 mA/load

These characteristics also apply to the PCT input described in paragraph 2.3.4.

Digital Programming Circuit Requirements. All digital programming inputs may be controlled by contact closures to ground (pin 24) since each circuit is provided with an internal 100 kΩ (5 kΩ for $\overline{RM}$) pullup resistor to restore the unconnected circuit to the "one" level. Except for $\overline{RM}$, faster pullup may be obtained by using an external pullup

Table 2-1
PROGRAMMING FUNCTIONS

Pin No.	Signal	Function Controlled	No Connection or One Level	Zero Level	Load Factor
1	$\overline{SG}$	MEAS RATE	both "1" = AUTO	FAST	1
2	$\overline{LG}$	MEAS RATE	both "0" not allowed	SLOW	2
3	$\overline{RM}$	RESET		RESET	1½
4	DTB	DISPLAY TIME	See paragraph 2.3.2 for circuit requirements		–
5	SLP	SLOPE	+ (positive)	– (negative)	1
6	DTA	DISPLAY TIME	See paragraph 2.3.2 for circuit requirements		–
7	1 MF	INPUT BAND	all "1" = 10 MHz more than two "0" is not recommended	1 MHz	1
8	100 KF	INPUT BAND		100 kHz	1
9	10 KF	INPUT BAND		10 kHz	1
10	1 KF	INPUT BAND		1 kHz	1
11	RTLA	TRIG LEVEL	See paragraph 2.3.2 for circuit requirements		–
12	+5	——	——		–
13	10X	PRESCALER FACTOR	both "1" = X1	X10	1
14	100X	PRESCALER FACTOR	both "0" not allowed	X100	1
15	TG2	EXT STD FREQ	1 MHz	100 kHz	2
24	GND	——			–

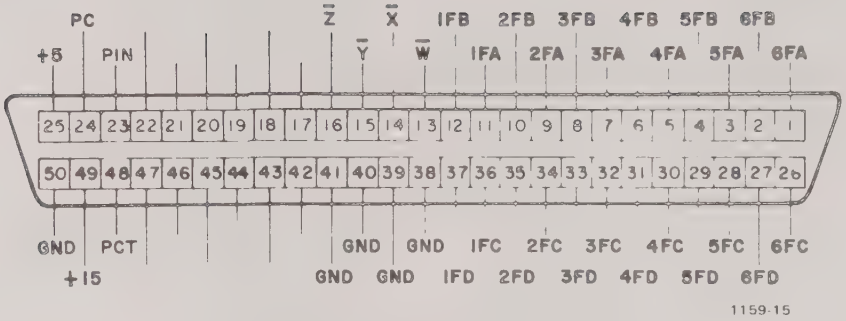


Figure 2-6. Data Output Connector.

Table 2-2
DATA OUTPUT CIRCUIT FUNCTIONS

Pin	Signal	Function		Function	Signal	Pin
1	6FA	1 bit, 6th digit	6th digit of readout	4 bit	6FC	26
2	6FB	2 bit, 6th digit	(least significant digit)	8 bit	6FD	27
3	5FA	1 bit	5th digit of readout	4 bit	5FC	28
4	5FB	2 bit		8 bit	5FD	29
5	4FA	1 bit	4th digit of readout	4 bit	4FC	30
6	4FB	2 bit		8 bit	4FD	31
7	3FA	1 bit	3rd digit of readout	4 bit	3FC	32
8	3FB	2 bit		8 bit	3FD	33
9	2FA	1 bit	2nd digit of readout	4 bit	2FC	34
10	2FB	2 bit		8 bit	2FD	35
11	1FA	1 bit	1st digit of readout	4 bit	1FC	36
12	1FB	2 bit	(most significant digit)	8 bit	1FD	37
13	W̄	1 bit	Decimal Point Position	4 bit	GND	38
14	X̄	2 bit		8 bit	GND	39
15	Ȳ	1 bit	Measurement Units	4 bit	GND	40
16	Z̄	2 bit		8 bit	GND	41
17						42
18						43
19						44
20						45
21						46
22						47
23	PIN	Printer inhibit input		Print command termination input	PCT	48
24	PC	PRINT COMMAND			+15V	49
25	+5V				GND	50

Table 2-3
RESISTANCE VALUES FOR DISPLAY TIME PROGRAMMING

Display Time	Approximate Resistance
.025 s	10 Ω
.050 s	200 Ω
.1 s	570 Ω
.25 s	1.7 kΩ
.5 s	3.5 kΩ
1 s	7.2 kΩ
2 s	14 kΩ
3 s	21 kΩ
5 s	32 kΩ
10 s	53 kΩ
∞	59 kΩ and higher

Table 2-4
DATA OUTPUT FORMAT

Decimal Digit	BCD			
	8-bit	4-bit	2-bit	1-bit
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

resistor or by driving with active circuits. Active pullup must not be used with RM since this circuit contains a "wired-OR" connection. An external pullup resistor may be used with RM, but short-circuit current should not exceed 10 mA.

Display Time Programming. Display Time is programmed by varying the resistance between DTA (pin 6) and DTB (pin 4) over a range of 0 Ω to about 60 kΩ. Table 2-3 gives approximate resistance values.

Trigger Level Programming. Trigger Level is programmed by an analog input voltage of −5 V to +5 V. This input gives the same range of adjustment as the front panel control with positive voltage corresponding to the − (negative) direction and negative voltage corresponding to the + (positive) direction. Input impedance is about 10 kΩ.

2.3.3. DATA OUTPUT CONNECTIONS.

Data Output Connector. The data output signals are connected to SO904, a 50-pin connector located on the instrument rear panel (see Figure 1-3); the connector mates with Amphenol P/N 57-30500. The wiring to the pins of SO904 from the instrument circuits is shown with associated signals in Figure 2-6.

2.3.4 Data Output Signal Characteristics.

Data Signal Characteristics. The data output circuits, pins 1 through 16 and 26 through 37, have the following characteristics:

"ONE" level voltage	5 V behind 6 kΩ
"ZERO" level voltage	0.45 V maximum
"ZERO" level current	−12 mA maximum

The data output format is 1-2-4-8 binary coded decimal, as defined in Table 2-4.

Table 2-5 lists the coding for the decimal point position (pins 13, 14, 38, 39) and measurement units (pins 15, 16, 40, 41).

Data Output Control Signals. The data plug contains three control signal circuits: "print command" output PC, pin 24; "printer inhibit" input PIN, pin 23; and "print command termination" input PCT, pin 48.

"Print Command" PC is a "ONE" level (positive) pulse or step which occurs at the end of the computation cycle to initiate the operation of a printer or other data output device. Its electrical characteristics are the same as the data output circuits described in paragraph 2.3.4 above. When no connections are made to PIN or PCT, the PC pulse is

Table 2-5
DECIMAL POINT AND MEASUREMENT UNIT CODING

Decimal Representation	BCD				Decimal Point Position	Units
	8-bit	4-bit	2-bit	1-bit		
1	0	0	0	1	after 1st digit	Hz
2	0	0	1	0	after 2nd digit	kHz
3	0	0	1	1	after 3rd digit	MHz

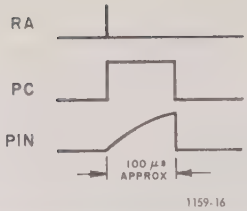


Figure 2-7. Waveforms when no connection is made to PIN or PCT.

about 100 μs wide (see Figure 2-7). By suitable connections to PIN or PCT the pulse may be increased to any desired width.

"Printer Inhibit" PIN is designed for use with instruments such as the 1137 printer, that provide a contact closure during the time that data are being read out of the data source. If PIN is grounded by the contact closure while PC is at the ONE level, PC will remain at the ONE level until after the PIN circuit is opened. The PC signal is used internally to inhibit generation of RC, thus preventing the data output from changing until the readout cycle is complete.

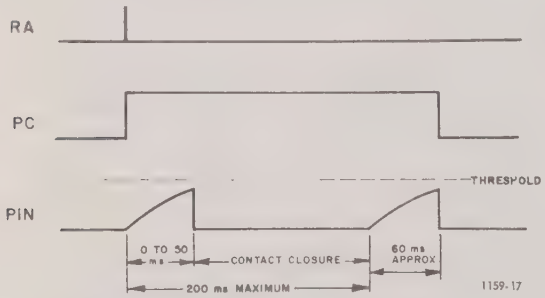


Figure 2-8. Waveforms when connected to 1137 Data Printer and a 6.8 μF external capacitor is connected to PIN.

It should be borne in mind, however, that the measurement logic is not inhibited. A new measurement may begin and be completed during the readout cycle if it is long enough. The new data will be held in the Time and Period Registers until the PC signal returns to its ZERO level, at which time the new frequency will be computed and made available at the data output. Figure 2-8 illustrates the waveforms and timing for connection to an 1137 Data Printer.

The basic 100-μs pulse width of the PC signal may be increased by adding capacitance between PIN and GND (pin 50). This must be done if the contact closure is delayed for more than 100 μs.

PC pulse width ≈ (.1 + 10 C) mS, C in microfarads

CAUTION

Active pullup must not be used with the PIN input.

"Print Command Termination" PCT is designed for use with instruments which provide a ZERO level to ONE level pulse or step when the readout cycle is complete. When PCT is used, there should normally be no connection to PIN. If PCT is at the ZERO level before the end of the 100-μs PC pulse, then PC will be held at the ONE level until the ZERO-to-ONE transition of PCT. Figure 2-9 illustrates the waveforms.

The PCT input may be driven from active circuits. Its input characteristics are the same as for the programming signals described in paragraph 2.3.2 and the load factor is 1.

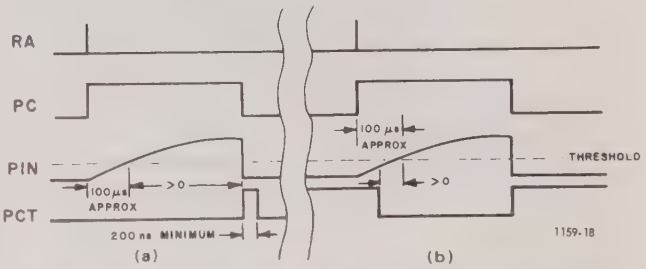


Figure 2-9. Waveforms when using PCT to terminate print command: (a) pulse (b) step.

2.3.5 Input and Output Jacks.

Signal Input. The INPUT jacks (J901 and J902) receive the signal frequency to be measured. The input sensitivity is typically 20 mV, rms, at 20 MHz, and 10 mV, rms, from 1 Hz to 10 MHz. The input impedance is 1 MΩ across 27 pF for up to 5 V peak-to-peak; 0.67 MΩ across 30 pF for up to 200 V peak-to-peak. Input capacitance can be reduced by disconnecting either unused front or rear panel input connector. Front only, 20 pF; rear only, 17 pF (see Figure 2-10).

External Reference Standard Input. An external reference standard signal can be connected to rear panel jack J903. The reference standard signal is either 1-MHz or 100-kHz of at least 1-V rms amplitude. General Radio's 1115-C Standard-Frequency Oscillator provides such a signal.

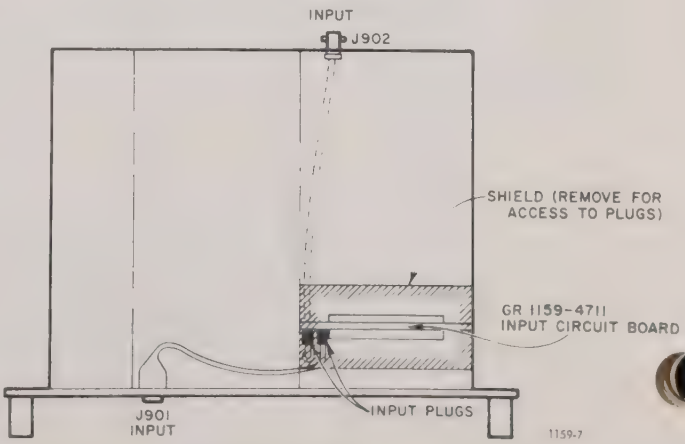


Figure 2-10. Input Board Plug Connectors.

Operation—Section 3

3.1 GENERAL.

The 1159 may be operated in either manual or programmed mode. The automatic features of the instrument reduce operating procedures to a minimum. See Figure 1-1 and 1-2 for locations of controls.

3.2 PRELIMINARY CHECKS.

a. Place POWER ON/OFF to OFF.

b. Check line switch S502 on the rear panel to correspond with the available line voltage (110-V ac or 220-V ac).

c. Unscrew fuseholders on rear panel and check that fuses of the proper value are installed (F501-0.8A, F502-0.4A).

d. Connect power plug (PL501) to primary power with line cord.

3.3 OPERATIONAL CHECK.

This paragraph describes operational check-out procedures to ensure proper function of the equipment.

3.3.1 Test Equipment Required.

The only equipment required for the operational check-out is a low frequency oscillator, such as a GR 1310 or equivalent.

3.3.2 Procedures.

a. Place rear panel PRESCALER FACTOR switch (S907) to X1 position.

b. Place MEAS RATE (S904) to FAST.

c. Place TRIG LEVEL (R901-S908) to mid-range.

d. The INPUT BAND switch (S905) is placed in the proper position to attenuate HF noise under adverse signal conditions. See the instrument specifications for range settings.

e. Place DISPLAY TIME (R902-S902) control to minimum.

f. Place POWER switch to ON. Allow a minimum warm-up time of 10 minutes. (A 10-minute warm-up period is required to attain the specified accuracy of the internal oscillator.)

g. Observe NO SIGNAL on front panel indicator (P904).

h. Adjust the test oscillator to an output frequency of 1 MHz with an amplitude of approximately 1 V rms.

i. Connect the oscillator to the frequency INPUT (J901, front panel or J902, rear panel) of the 1159 using suitable connectors and cable.

j. Observe the neon readout indicators for a reading of about 1.00000 MHz and observe that the NO SIGNAL indicator is de-energized.

k. Change the oscillator frequency to 10 Hz. Slowly decrease the frequency and observe that the LOW FREQUENCY indicator (P905) is energized at approximately 6-Hz and below.

l. Place MEAS RATE switch (S904) to SLOW. Observe that LOW FREQUENCY INDICATOR (P905) is de-energized.

m. Place MEAS RATE switch (S904) to AUTO. Slowly change the oscillator frequency from 2 Hz to 20 Hz and observe the readout indicator for proper frequency. Note that the LOW FREQUENCY indicator does not energize.

n. Adjust DISPLAY TIME (R902-S902) control fully ccw. Rotate slowly cw through the entire range and observe that the display time increases from very short duration (actually 0.02 s) to very long (10 s) and ultimately to infinity.

o. With DISPLAY TIME at infinity (HOLD) push the RESET button (S901) and observe a reset to zero on all indicators, followed by a recomputation and display upon release.

3.4 MANUAL OPERATION.

a. Place POWER switch (S501) to ON. Allow a minimum warm-up time of 10 minutes.

b. Connect signal to be measured to INPUT jack (J901 or J902) on front or rear panel, respectively.

c. Place SLOPE switch (S903) to + or — for trigger slope desired.

d. Place MEAS RATE switch to FAST, SLOW or AUTO as required by signal conditions.

NOTE

If a wide range of signal frequencies is being scanned the AUTO position automatically switches clock speed as required.

e. Adjust TRIG LEVEL to the proper polarity and threshold required for signal triggering.

NOTE

This adjustment is only required for low level pulse signals. No adjustment is required for normal high level signals.

f. Select the appropriate filter with INPUT BAND switch (S905) as required by the input signal frequency.

NOTE

The INPUT BAND switch is required when noise on the signal causes a reduction in accuracy, as evidenced by abnormal fluctuations in the readout or erratic operation. The −3-dB points for each switch setting are listed in the instrument specifications.

g. Adjust the DISPLAY TIME control (R902-S902) as desired.

h. Place PRESCALER FACTOR switch (S907) on rear panel to X1 for signals from 0.6-Hz to 20-MHz, to X10 when using a 10:1 scaler, and to X100 when using a 100:1 scaler preceding the input. The instrument is direct-reading in these cases, and requires no operator conversion.

i. Place EXT STD FREQ switch (S906) in the proper position to correspond to the external standard frequency being used (1-MHz or 100-kHz). If no external standard frequency is supplied, the switch may be left in either position.

3.5 PROGRAMMED OPERATION.

a. Connect the programming device to the PROGRAMMING INPUT connector (SO905) on the instrument rear panel.

b. Place SLOPE switch (S903) to +R position.

c. Rotate TRIG LEVEL (R901-S908) fully cw to REMOTE position.

d. Place INPUT BAND switch (S905) to 10-MHz-R position.

e. Rotate DISPLAY TIME (R905-S902) fully cw to HOLD-R position.

f. Place MEAS RATE switch (S904) to AUTO-R position.

g. Place EXT STD FREQ switch (S906) to 1-MHz (REMOTE) position.

h. Place PRESCALER FACTOR switch (S907) to X1 (REMOTE) position.

i. Operate by remote programming in the same manner as manual operation, except POWER ON/OFF.

Theory–Section 4

4.1 INTRODUCTION

4.1.1 General.

The 1159 counter measures the time of one or more input frequency periods. A built-in computer stores the time and period quantities in their respective registers during the count operation cycle. When the information is properly stored a compute operation cycle is initiated by logic circuits. An arithmetic program computes the quotient of the number of periods per unit of time and stores the (frequency) information in the quotient registers. The Quotient Register decade counter units (DCU's) provide 1-2-4-8 BCD information to decimal decoder/driver units in the display section. The frequency information is displayed on neon-display indicators. The Quotient Register DCU's also provide BCD information to a data output connector for use with external devices.

The frequency information is displayed properly scaled and may be read directly. Additional indicators display the proper unit of frequency (Hz, kHz, MHz) and furnish a visual indication if the frequency is too low to be measured or if there is no signal present.

4.1.2 Basic Operating Theory.

See Figure 6-1, Block Diagram. A stabilized 10-MHz Clock Oscillator generates the timing information to measure input frequency periods. The clock furnishes either a 10-MHz signal or a 1-MHz signal to the time register. The clock speed may be shifted manually by a panel switch, or automatically, allowing instrument logic to select the proper speed for the frequency being measured. The frequency to be measured is applied to the input circuit where it is amplified and applied to a Schmitt trigger. Conditioning circuits shape the Schmitt output into a pulsed count signal that is applied to the Gate circuits. The first pulse of a measurement enables the Gates to apply the clock signal to the time register and the input-frequency count signal to the period register. Logic circuits compare the time and period register information to generate a stop signal, after an appropriate period of time, to allow the gates to be closed by the next signal pulse.

When the count cycle is stopped, gating functions initiate the compute cycle. The Arithmetic Program circuit performs arithmetic operations on the information from the time and period registers. The time and period information is shifted out of the registers into the Arithmetic Program circuits and the result of the arithmetic operations is reloaded into the registers by shift pulses generated in the Add Cycle and Reset circuits. The basic process consists of subtracting the time information from the period information (in two's complement notation) until no carry is generated. The number of carriers generated at the completion of each subtraction is applied to the most significant digit of the Quotient Register. The contents of the time register is reloaded with the same information at each arithmetic operation and is then added to the remainder in the period register. The sum is retained in the period register, multiplied by 10, and reloaded into the period register. Now the subtraction process is repeated to load the next significant digit of the Quotient Register. The process is repeated until all six significant digits of the Quotient Registers are loaded and a round-off computed. Decade counters in the Quotient Registers apply 1-2-4-8 BCD information to decoder/drivers in the display section. The decoder/drivers convert the BCD information to decimal outputs for the neon-display indicators. After the round-off digit has been computed, a display signal is generated to the display indicators. The duration of the display is determined by a panel control. At the end of the display, the Reset circuits initiate another count cycle.

Range Counter circuits determine the proper placement of the decimal point and compute the proper frequency unit. Circuits in the Range Counter drive visual indicators when the frequency being measured is too low for the instrument to measure at either clock speed. A visual indication also warns when there is no input signal present.

4.2 SPECIAL LOGIC CIRCUITS.

A thorough knowledge of the ground rules for logic elements is necessary for the subsequent discussions of circuit analysis and trouble analysis. A positive-logic scheme is used throughout the Type 1159, i.e., the ONE level is a more positive potential than the ZERO level.

4.2.1 AND Gate.

The output of the AND gate is up (ONE level) only when all inputs are also up.

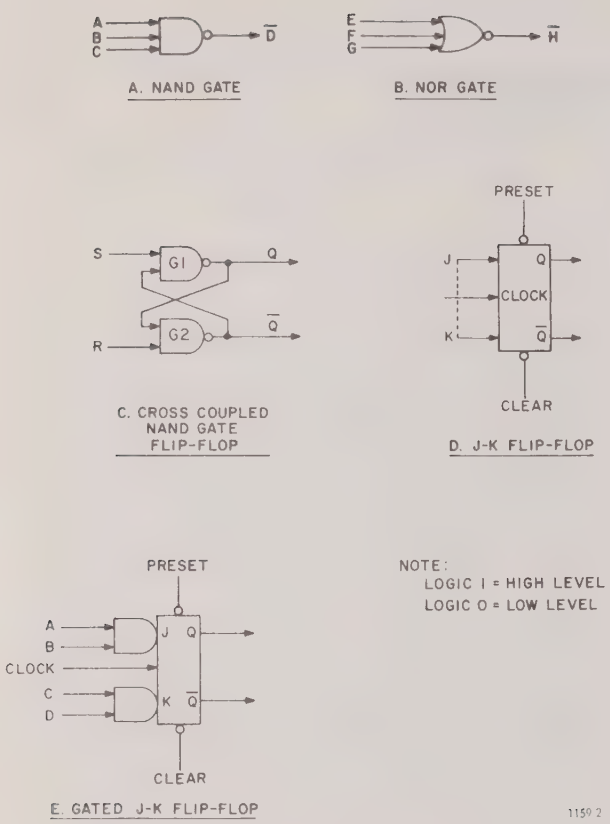


Figure 4-1. Basic Logic Symbols.

4.2.2 NAND Gate.

The NAND gate (Figure 4-1A) produces a ONE output when any or all inputs are ZERO. Conversely, the output is a ZERO only when all inputs are ONE.

4.2.3 NOR Gate.

The NOR gate (Figure 4-1B) output is ZERO when any or all inputs are ONE; a ONE output results only when all inputs are ZERO.

4.2.4 Cross-Coupled NAND Gate Flip-Flop.

Figure 4-1C illustrates a cross-coupled NAND gate flip-flop comprised of two NAND-gate elements. This type flip-flop normally requires a ONE input on both the SET and RESET inputs to maintain the output state. The output state is changed by applying a ZERO to either input.

Assume a ONE input at S and R, a $\overline{Q}$ output of ONE, and a Q output of ZERO. To change the state of the flip-flop (i.e., produce a ZERO Q output and a ONE $\overline{Q}$ output), let us apply a ZERO to S. This input switches Q to a ONE, and, of course, the cross-coupled input to G2. Since R is already ONE, both inputs to G2 are now ONE, and $\overline{Q}$ becomes ZERO. Since $\overline{Q}$ and S are both ZERO, Q is maintained at the ONE level.

4.2.5 J-K Flip-Flop.

The J-K flip-flop (Figure 4-1D) is used extensively in divider circuits. The flip-flop has a clock input that switches the state of the flip-flop when both the J and K inputs are enabled. The J and K inputs may be tied to the clock input to enable operation as a toggle flip-flop. If the J and K inputs are enabled by external gating signals, the flip-flop will change state only when the proper input is enabled. A ONE level is required to enable the J and K inputs; the PRESET and CLEAR inputs are activated by a ZERO level. The ONE PRESET input sets the flip-flop so that the Q output is the more positive; a ONE at CLEAR resets the flip-flop so that $\overline{Q}$ is the more positive output.

The Gated J-K flip-flop (Figure 4-1E) operates in a similar manner, except that two or more ONE signals are required to enable the J and K inputs.

4.2.6 Full Adder Logic.

A series full adder is used in the 1159 counter to perform arithmetic operations on the contents of the time and period registers to compute frequency measurements.

The following discussion analyzes the logic theory of the basic adder configuration used in the 1159 and is keyed to Figure 4-2.

The adder can be considered in terms of its two major sub-sections (Figure 4-2): the forward carry area (A1, A2, A3, etc) and the sum group (A4, A5, etc). Both of these areas consist of several two-input AND gates (except A7) and a multiple-input NOR gate. The lower set in the figure produces the sum; the upper set produces the forward carry. The forward carry is sorted in a J-K flip-flop and reapplied to the adder input as the low-order previous carry for the next serial addition.

The addend (A) and augend (B) are applied to NOR gates I_1 and I_2 inverted to $\overline{A}$ and $\overline{B}$ and applied to the adder input AND gates. NOR gates O_1 and O_2 invert the logic and generate forward carry and sum information respectively. The flip-flop stores forward-carry information for the next addition. The output of NOR gate O_1 is applied to the gate inputs of the SUM gate circuits as the low-order carry.

Simplified Functional Theory. The adder logic displayed in Figure 4-2 may be stated by the following Boolean expressions:

a. Carry (A1, A2, A3, O_1).

$$\overline{(\overline{A}\cdot\overline{C}) + (\overline{A}\cdot\overline{B}) + (\overline{B}\cdot\overline{C})}$$

b. Sum (A4, A5, A6, A7, O_2).

$$\overline{(\overline{A}\cdot D) + (\overline{B}\cdot D) + (\overline{C}\cdot D) + (\overline{A}\cdot\overline{B}\cdot\overline{C})}$$

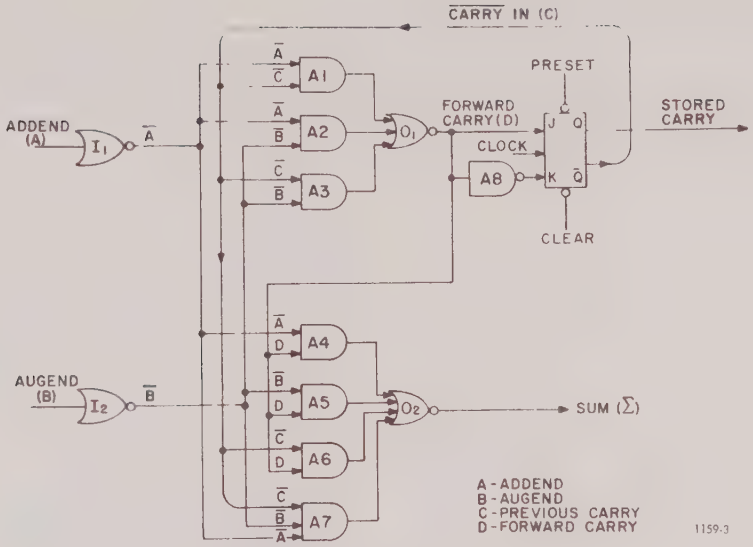


Figure 4-2. Full-Adder Logic.

These expressions simplify to the following:

a. Carry

$(A+C) \cdot (A+B) \cdot (B+C)$

b. Sum

$(A+\overline{D}) \cdot (B+\overline{D}) \cdot (C+\overline{D}) \cdot (A+B+C)$

The simplified expressions are illustrated in Figure 4-3.

The following discussion of basic full adder operating theory is keyed to Figure 4-3.

Add-No Carry. Refer to column 2 of the full adder truth table on Figure 4-3. The addend (A) is a ONE applied to OR gates 1, 2, 4 and 7. The augend (B) is a ZERO applied to OR gates 1, 3, 5 and 7. Carry in (C) is a ZERO (no low order carry) applied to OR gates 2, 3, 6 and 7. Therefore gate 1 output is ONE; gate 2 ONE; and gate 3 ZERO. The forward carry (D) output of AND gate 8 is ZERO (no forward carry).

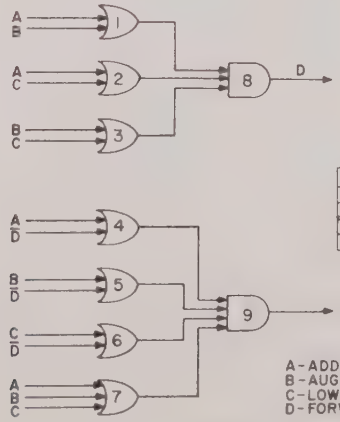
The output of OR gate 4 is ONE; gate 5 is ONE (complement of carry ZERO); gate 6 is ONE; and gate 7 is ONE. The SUM output of AND gate 9 is ONE.

This corresponds to the truth table (column 2) where with A=1, B=0, C=0; SUM = 1 and D=0.

Add-Forward Carry. Refer to column 5 of the truth table on Figure 4-3. In this example, the addend (A) and augend (B) are both ONE. OR gates 1, 2 and 3 all have a ONE output. AND gate 8, therefore, generates a carry (D) output of ONE.

OR gates 4, 5 and 7 are all ONE outputs. OR gate 6 has a ZERO output (C = 0, $\overline{D}$ = 0). The SUM output of AND gate 9 is ZERO. This corresponds to truth table column 5 where with A = 1, B = 1, C = 0; SUM = 0 and D = 1.

The remaining columns of the truth table follow in the same manner.



FULL ADDER TRUTH TABLE

	1	2	3	4	5	6	7	8
ADDEND (A)	0	1	0	0	1	1	0	1
AUGEND (B)	0	0	1	0	1	0	1	1
LOW ORDER CARRY (C)	0	0	0	1	0	1	1	1
SUM	0	1	1	1	0	0	0	1
FORWARD CARRY (D)	0	0	0	0	1	1	1	1

Figure 4-3. Simplified Full-Adder Logic.

4.3. DETAILED LOGIC DESCRIPTION.

The following overall detailed logic description is keyed to Figure 6-2, over-all logic and timing diagrams, with key logic components called out wherever practicable.

4.3.1. Clock Circuit.

The time base for the Clock Circuit is a 10-MHz crystal-controlled, stabilized oscillator. The shaped oscillator output of 10 MHz is applied to NAND gate IC 607C and to a decade divider (IC 602). A 5-MHz output(from the first binary element of the decade) provides a clock signal (CA) that is used as the timing for compute-cycle operations. The 1-MHz output of IC602 is applied to IC 607B as the slow-speed clock signal, to IC 605C in the phase detector, and to a second decade divider (IC 603). The 100-kHz output of IC 603 is applied to IC 605D of the phase detector.

Phase Detector. An external reference standard of either 1 MHz or 100 kHz may be selected to phase-lock the clock oscillator. The external reference input is applied to one input of a flip-flop. The EXT REF SELECT switch (S906) is placed in the position corresponding to the external reference frequency (1 MHz or 100 kHz). The EXT REF SELECT switch enables either IC 605C or IC 605D, which applies the corresponding oscillator frequency to the other input of the phase detector flip-flop. The phase difference between the external reference and the oscillator frequency generates a dc voltage which is applied to a varicap in the tuned circuit of the oscillator, effecting a phase lock.

Clock Selection Logic. Output signals from the time register are received by IC 608B and applied to the clock selection logic. Output NQ4 from the period register is also applied to the clock selection logic. If an output from gate IC 608B is received, an overflow of the time register is indicated, signifying that the slow clock speed (1 MHz) is required. An output from NQ4 indicates a frequency high enough to be measured at the fast (10-MHz) rate. The clock-selection logic enables either IC 607C (10 MHz) or IC 607B (1 MHz) according to the requirements. Signal G from the Gate Circuit determines the duration of the count cycle. The output of IC 604A is either a 1-MHz or 10-MHz clock signal (CT) to the ripple counter input of the time register.

4.3.2 Input Circuits.

The frequency to be measured is applied to the input jack (J901 or J902). The input circuits consist of FET amplifier low-noise stages that amplify the signal, a Schmitt trigger and pulse-shaping circuits. Filter circuits in the amplifier are controlled by a panel switch and are selected to filter high-frequency noise from the signal. A trigger-level control is used for low-amplitude pulse signals and output trigger slope (+ or –) may be selected. The trigger output signal (CN) is applied to the gate circuits.

4.3.3 Gate Circuits.

The frequency to be measured (CN) from the input board drives the clock input of flip-flop IC157, the J input of which is enabled by a flip-flop at the end of the display cycle. The CN signal sets IC157 to the Q state to start the count cycle and the Q output is the gate signal (G) that is fed to the Clock Circuit and to IC158C/D. The CN signal is now gated from IC158C/D as the signal CNG to the period register ripple-counter input.

Stop Logic. The stop-logic circuits receive signals from the time and period registers and respond to any one of four predetermined count combinations. Upon recognition of one of these combinations, the stop logic applies an enabling gate to the K input of IC157. Signal CN resets the flip-flop to the $\bar{Q}$ state, disabling gate signal G and stopping the count.

4.3.4 Time and Period Registers.

The 10 MHz/1 MHz clock output (CT) drives the first flip-flop of a 24-stage binary ripple counter. The Time Register will accumulate clock pulses until the count is stopped by the stop logic. At the same time that the Time Register accumulates clock pulses, the Period Register is counting and accumulating input frequency pulses (CNG). The Period Register is also a 24-state binary ripple counter identical to the time register. When the count cycle is stopped, the compute cycle is started. During the compute cycle shift pulses are fed to each stage of both registers. By means of gating, the Time and Period Registers now function as shift registers. The accumulated time information is shifted out of the register from the Q1 and $\bar{Q}1$ outputs of the first stage to the Arithmetic section. As the information is shifted out of the Time Register to the Arithmetic section, it is also reloaded into the 24th stage and shifted back toward stage one. A series of 24 shift pulses is generated for each arithmetic function, so that the information in each of the 24 stages is applied to the arithmetic section. When the 24-shift-pulse cycle ends, the Time Register will be reloaded with the original time information for the next arithmetic function.

The accumulated information is shifted from the Period Register by the shift pulses in the same manner as for the Time Register except for reloading. The information from the Period Register is applied to the Arithmetic Section for processing in a full adder. The sum information from the arithmetical process is loaded back into stage 24 of the period register and shifted back to stage 1 by the 24 shift pulses.

4.3.5 Arithmetic Program.

The Arithmetic Program section performs computations on the contents of the time and period registers and generates frequency information that is stored in the Quotient Registers.

The Arithmetic Program sequence generator consists of flip-flops IC408A (subtract), IC407B (add), IC407A (multiply) and IC406A (recycle). During the count cycle, IC406A remains set in the Q state. The Q output of IC406A enables the J input of IC408A. No CP pulses from the add cycle and reset section are received, however, during the count cycle. When the stop logic ends the count cycle and enables the compute cycle, a CP pulse is generated that resets IC406A to the $\overline{Q}$ state, sets IC406B to the Q state and sets IC408A to the Q state. The Q output of IC408A is applied to AND gates 1 and 4 of the AND/NOR gate inputs to the full adder. The Q output of IC408A is also applied as an enabling input to IC410A. The subtraction process is now enabled. The period register output (NQ1) is applied to AND-gate 1, and the complemented time register output ($T\overline{Q1}$) is applied to AND-gate 4. The shift pulses apply the 24 bits of each register to the adder for the subtraction process.

Subtraction. By using the complement of the Time Register and adding it to the contents of the Period Register and the preset carry, the program subtracts the time quantity from the period quantity by two's complement addition. If the period quantity is greater than the time quantity, a carry is generated at completion of subtraction. The carry output of IC406B is gated to the Quotient Registers by pulse CP at the end of each subtraction. The sum output of the adder (difference) is loaded back into the Period Register. The Arithmetic Program continues to subtract the time quantity from the remainder in the Period Register until no carry is generated. When there is no carry, IC406B is in the $\overline{Q}$ state, enabling IC410C. The next CP pulse resets IC408A to the $\overline{Q}$ state, disabling the subtract operation.

Addition. The J input of IC407B is enabled by IC410C and is set to the Q state. The Q output of IC410B is applied to AND gates 2 and 5 in the adder input gates. The adder now adds the Time Register quantity (TQ1) and the Period Register quantity (NQ1) that is the remainder from the subtract operation. The sum is loaded back into the Period Register. The next CP pulse is applied to IC405D that is enabled by the Q output of IC407B. Carry flip-flop IC407B is reset to the $\overline{Q}$ state by IC405D. (Although not shown in Figure 6-2, the multiply-by-10 flip-flops, IC409A, IC409B, and IC408B, are also reset to the $\overline{Q}$ state by IC405D.) At the same time, IC407B is reset to the $\overline{Q}$ state and IC407A is set to the Q state. The Q output of IC407A is applied to AND gates 3 and 6 of the adder input circuit.

Multiplication. The adder now performs a multiply-by-10 operation on the contents of the Period Register. This is accomplished by flip-flops IC409A, IC409B and IC408B which are, in effect, three additional stages to the Period Shift Register. Adding a stage at the end of the register has the effect of multiplying the quantity in the Period Register by two. The Q output of IC409A is applied to AND gate 6 and the Q output of IC408B is applied to AND gate 3 of the adder input. The adder sums the quantity (Q) multiplied by two with the same quantity multiplied by 8.

EXAMPLE

$$2Q + 8Q = 10Q$$

$$(Q = 4)$$

$$2 \cdot 4 + 8 \cdot 4 = 10 \cdot 4 = 40$$

The adder sum is loaded back into the Period Register. The Arithmetic Program is now ready to begin the next subtract function to load the Quotient Register for the next digit.

End of Arithmetic Program Cycle. The next CP pulse resets IC407A to the $\overline{Q}$ state, thereby disabling the multiply function and sets IC406A to the Q state. The Q output of IC406A enables the J input of IC408A, which generates a Q output to enable the adder input for the next subtract operation.

NOTE

The preceding description of the Arithmetic Program cycle (subtract-carry, add, multiply X 10) is for loading one digit of the Quotient Register. The process is repeated six additional times (not counting left-hand zeros) to load all six digits and compute the round-off digit. The Quotient Registers are loaded only by subtract operation carries. Add and multiply operations prepare the quantity for the next significant decimal display number.

The Q and $\overline{Q}$ outputs of IC406A also furnish signals DC and $\overline{DC}$, used for gating in the add cycle and reset section.

4.3.6 Add Cycle and Reset.

The Add Cycle and Reset section generates shift pulses (CS), the arithmetic program cycle pulse (CP), the reset signals (RA and RC) and the print command ($\overline{PC}$).

The shift pulses (CS) and cycle pulses (CP) are generated by a divide-by-32 counter. The clock-input counter drive is at a 5-MHz rate (CA) from the Clock section. The counter is enabled by IC455D. During the count-cycle signals DC and QC are at a ONE level causing IC455D to produce a ZERO output. The ZERO output of IC455D inhibits the J and K inputs to the counter input, disabling the count.

At the end of the instrument count cycle, reset C (RC) is generated, initiating the compute cycle. Reset C (RC) causes signal QC to drop to a ZERO level, generating a ONE

output from IC455D. The divide-by-32 counter is now enabled and starts counting. The counter is preset with all stages in the Q (ONE) state. AND gate IC461 has a ONE input from Q2 and a ZERO input from signal $\overline{DC}$, generating a ZERO output to NOR gate IC461. The Q1 output to IC461 is ONE; $\overline{Q3}$ is ZERO. The Q4 and Q5 outputs are a ONE level to IC455C. The ZERO output of IC455C is applied to NOR gate IC461, which has three ZERO inputs and one ONE input for an output of ZERO. When the first clock pulse resets Q1 to a ZERO, NOR gate IC461 now has all ZERO inputs and generates a ONE level output pulse (CP). Gate IC455C generates a ZERO inhibit level to IC455B. The second clock input causes all flip-flops in the divide-by-32 counter to reset to ZERO. Gate IC455C now generates a ONE output (GCS) that enables IC455B. Signal CA (5 MHz) is now gated through IC455B as the shift-pulse signal ($\overline{CS}$). Twenty-four shift pulses are gated until Q4 and Q5 go to a ONE level at clock time 26. Signal GCS drops to a ZERO level inhibiting the shift pulses ($\overline{CS}$).

The divide-by-32 counter continues to generate shift-pulse groups (CS) and the cycle pulse (CP) until the last Quotient Register is loaded. When the Quotient Register divide-by-5 round-off register is enabled, signal QC rises to a ONE level. When the Arithmetic Program sequence generator completes its last sequence, signal DC rises to a ONE level. Gate IC455D now generates a ZERO level inhibit output to the J and K inputs of the counter and stops the count. The ZERO output of IC455D also generates the reset A (RA) pulse that resets the counter and other instrument circuitry to initiate the display/count cycle.

Reset C (RC) is generated at the end of the count cycle by signal $\overline{G}$ which drops to a ZERO level. Reset C (RC) initiates the compute cycle.

4.3.7 Quotient Registers A and B.

Quotient Registers A and B contain gating circuits and decade counter units (DCU's) that convert digital-frequency information to 1-2-4-8 BCD quantities for each of the six decimal-display indicators. The Quotient Register A board contains circuits for the three most significant digit registers (1, 2, 3). Quotient Register B contains circuits for the three least significant digit registers (4, 5, 6) and the round-off register. At the beginning of the compute cycle, reset C (RC) resets the Quotient Registers (flip-flops and DCU's) to the ZERO state. Signal $\overline{RC}$ sets IC256B/C to the Q state, enabling IC256D. Frequency information is gated via IC256D and IC256A into the DCU for display unit 1. The frequency-information pulses (CF) are generated by the CP pulse, and carry, gated by the subtract function in IC410A. At the end of an Arithmetic Program cycle, signals DC and CP generate signal $\overline{CD}$ from IC405A, which is applied to IC260A. The inverted output (CD) is applied to the gate flip-flops (IC254A/B, IC301A/B and C, IC308A/B) as the clock pulse. When the Arithmetic Program cycle has loaded the most significant DCU, a ONE output is produced at gate IC257B, which enables the input of flip-flop IC254A. A CD pulse then sets flip-flop IC254A to the Q state and resets flip-flop IC256B/C to the $\overline{Q}$ state. The Q ONE level output of IC254A gates CF pulses to the second DCU, via IC255D and IC255A and enables the J input of IC254B. Any carry from the second DCU is coupled back to the first DCU via IC256A. When the second DCU is loaded and the second program cycle ends, a DC pulse sets IC254B to the Q state, which loads the 3rd (less significant), DCU via IC255B and IC255C. The process continues until all six DCU's and the divide-by-5 round-off register are loaded. If a carry occurs from the round-off register, it propagates to the more significant DCU's. When IC308B enables IC310A, the Q output is also applied to the add cycle and reset section as signal QC. Signal QC is NANDed with signal DC (at the completion of the last program cycle to end the computation) and generates a display gate.

The DCU (1-2-4-8 BCD) outputs are applied to decoder/drivers in the Display.

4.3.8 Display.

The Display section contains the decoder/drivers and the 6 neon-display indicators.

The DCU outputs from the Quotient A and B Registers are applied to the six decoder/drivers in the Display section. The 1-2-4-8 BCD outputs of the DCU's are decoded to provide 10 exclusive outputs to each neon indicator. The BCD input reads out as a decimal equivalent on the display indicators. The readout is to six places; indicator 1 is the most-significant number and indicator 6 the least significant.

4.3.9 Range Counter.

The Range Counter section computes the proper unit of frequency for a direct readout. Logic circuits also drive visual indicators when no input signal is present and when the input frequency to be measured is too low at the selected clock speed.

Frequency Units. The frequency units are identified by decimal-point placement and by visual indicators (Hz, kHz or MHz). Provisions are also made for direct readout with either a 10:1 or 100:1 prescaler. The prescaler factor is selected by a panel switch (S907). The switch selects a factor of X1, X10 or X100 which gates the preset logic circuits. Signal 10MG gates the logic for fast or slow clock speed. The preset logic presets the two divide-by-3 counters for proper unit scaling. The divide-by-3 counters are clocked by the CD clock pulse from the Arithmetic Program section. Pulse CD occurs at each Arithmetic Program cycle completion. One of the counters drives the decimal point indicators and the other counter drives the frequency unit (Hz, kHz, MHz) indicators. The preset logic always generates a proper direct readout for input frequencies within the range of the instrument.

Low Frequency/No Signal. When the input-signal frequency is too low to be measured at the selected clock

speed, logic circuits energize the LOW FREQ indicator on the front panel.

Reset C ($\overline{RC}$) resets the LF logic to a normal state. When a low frequency condition exists, signal $\overline{TOF}$ (time-register overflow) sets the logic circuitry to provide an output drive to the LOW FREQ indicator when signal $\overline{G}$ (from the Gate, not shown on Figure 6-2) is ZERO (count cycle). If the input frequency is too low for the fast-speed clock (10 MHz), the clock speed is switched to slow (1 MHz). If the frequency is too low for the slow clock speed, the LOW FREQ indicator will remain lighted.

The NO SIGNAL logic is gated by the start signal ($\overline{STG}$). The $\overline{STG}$ signal is normally a ONE level and goes to a ZERO level pulse of one input frequency time period in width. A time constant circuit prevents the NO SIGNAL indicator from energizing during this pulse width. If, however, no signal is present, $\overline{STG}$ remains at a ZERO level. The time delay is equal to slightly more than one machine cycle and then the NO SIGNAL indicator energizes.

4.4 CIRCUIT DESCRIPTIONS

This section describes the operational theory of each module and identifies the input and output signals. A schematic and/or logic diagram of each module is included in Section 6 of this manual. A signal index in Section 6 lists the signal mnemonics and their functions.

4.4.1 Power Supplies (Figure 6-4).

+5-V dc Regulated: The +5-V dc power supply is series regulated with an adjustment to calibrate the output voltage level and is designed with protection against short-circuit overloads.

A full-wave bridge rectifier and filter circuit supply unregulated negative dc to the emitters of Q501 and Q502, the series-regulator transistors. Q501 and Q502 are compound-connected for linear current amplification. The regulated +5-V dc collector output is applied across a voltage divider, consisting of R503 and potentiometer R502. The divided output voltage is compared with the Zener reference voltage (CR508) by Q505 and the error signal is further amplified by Q503. Q504 acts as a base current source to the series-pass transistors. The amplified error current is shunted away from the base of Q502, providing the regulation. The output current is sampled by R508, in parallel with R513. When a current overload occurs, the voltage developed across this resistor is greater than 1.1-V; Q503 is turned on, preventing any further drive to the series transistors and limiting the output current.

The details of the circuit functions are as follows. An increase in output voltage applies a more negative bias to the base of Q505, causing it to increase conduction. This increase in current is further amplified by Q503. When Q503 increases conduction, it shunts current away from the base of Q502, causing it to decrease conduction. The resulting decrease in current through the output load drops the voltage to its proper level. Q501 is compound-connected with Q502 for linear current amplification.

+ and −15-V dc Regulated: The regulated −15-V dc supply is comprised of Q555—Q558, and is the reference for regulating the +15-V dc supply. The error amplifier, Q558, has the emitter stabilized by a Zener voltage reference circuit, CR564 and C556. The base of Q558 is connected to a potentiometer, R569, that is in a voltage divider connected across the −15-V dc supply. The output voltage is adjusted to the proper value by R569. The error amplifier controls the base current of Q556, which in turn controls the base current of series regulator Q555. A current over load causes Q556 to conduct more heavily as in the overload protection of the 5-V supply, thus limiting the output current.

The operating principles of the −15-V dc supply are as follows. Assume that the output voltage is tending to decrease to a less negative value. A less negative voltage is sensed at the base of Q558, decreasing conduction, which in turn decreases the conduction of Q556. The base current of Q555 series regulator now rises, causing the series current to increase, which restores the output voltage to a more negative value.

The +15-V dc supply uses the −15-V dc regulated supply as a reference and does not have a separate calibrating adjustment. It is comprised of the Q554 and Q552 error amplifiers, the Q551 series regulator, and the Q553 current source. Q554 and Q553 emitters are driven by the −15-V dc regulated supply. The base of Q554 is tied to a voltage divider between the +15- and −15-V dc supplies. Any tendency for the +15-V dc output to change is sensed by Q554, and is regulated in the same manner as described for the −15-V dc supply, except that components have been selected for a positive power supply.

4.4.2 Crystal Oven and Control.

See Figure 6-5. The oscillator crystal is contained in a proportionally controlled oven with a heating element and a sensing thermistor. The thermistor is the R_x component of a resistive bridge that is connected across +15-V dc and ground. The bridge output is connected to a differential amplifier whose output is amplified to supply current to the oven heater. Temperature stability is achieved by feedback to the differential amplifier.

A differential amplifier (Q651/Q652) is connected across the output of a resistive bridge, (R654, R655 and R651, oven thermistor). The oven thermistor has a negative temperature coefficient. Assuming an increase in oven temperature, the thermistor decreases in resistance. This causes the bias at the base of Q651 to decrease. Q651 decreases conduction allowing the collector voltage to rise. This positive change is coupled to the base of Q653, which also decreases conduction, causing its collector voltage to decrease. This negative-going change at the base of emitter-follower Q654 decreases the collector current to the oven heater causing a

decrease in temperature. Stability is achieved by negative feedback from Q654 collector through R658 to the base of Q651 in the differential amplifier.

4.4.3 Input Circuit Board.

Input and Trigger Circuits. See Figure 6-6. The Input board consists of input amplifiers and shaping circuits, low-pass filter circuits, and the slope circuit.

The input signal to be measured is applied through coaxial cables from the front- or rear-panel jacks to jacks mounted on the circuit board. It is coupled through C101 to a symmetrical limiting circuit (R102, C102, CR101–CR104 that limits high-level inputs to approximately 1.4 V at the input to Q101. Q101 and Q102 form a feedback amplifier. Q101 is a field-effect transistor chosen for its properties of low noise and high input impedance. The output of Q101 is applied to the base of Q102. The emitter of Q102 is held at approximately 10 V by Zener diode CR105, while the collector load resistor is returned to −15-V dc. R105, R106 and C115 comprise the feedback network. The output at the collector of Q102 is capacitively coupled to a second stage comprised of a limiting circuit (R108, C103, C120, C122, CR106, CR107) and a feedback amplifier (Q105 and Q106) that operates identically to the first stage. The output of Q106 is capacitively coupled to a third limiter and amplifier stage (Q109 and Q110). This stage contains the trigger-level adjustment. The trigger level is adjusted by panel control (R901–S908) TRIGGER LEVEL ± that provides up to ±5-V dc to the base of Q115. Q115 operates as a variable current source, which adjusts the bias current of Q110 to effect a change in the quiescent output level of Q110 of about ±2 V, which represents over ±20-mV referred to the input. The trigger threshold level may also be externally programmed by a ±5-V dc signal (RTLA). The trigger-level zero-balance adjustment is controlled by potentiometer R125 in the FET drain circuit.

Filter Circuits. Switched low-pass filters are controlled by panel INPUT BAND switch (S905).

A pair of filters consisting of gate IC101B/Q103 and gate IC101C/Q104 is connected to the input circuit of Q105. Another pair of filters consisting of gate IC101D/Q107 and gate IC101E/Q108 is connected to the input circuit of Q109. Switch S905 applies a ground ZERO level in various combinations to the filter NAND gates as follows:

Bandpass	Filter
1-kHz	1 KF, 10 KF
10-kHz	10 KF, 100 KF
100-kHz	100 KF, 1 MF
1-MHz	1 MF
10-MHz	No filters

A ZERO level signal is applied to a particular filter NAND gate (IC101B–IC101E). The inverted ONE level output is applied to the base of its NPN transistor causing it to switch ON. The transistor switch connects a capacitor from the particular input circuit to ground, filtering out high-frequency noise and passing the lower-frequency signal. Band-switching may also be accomplished by programming inputs.

Schmitt Circuit. The output of Q110 is applied to a current-mode Schmitt trigger that provides a very sharp rise and fall time. Voltage translation is effected by Q112 and Q113.

Slope Circuit. The Schmitt-trigger output of Q113 collector is applied to the slope circuit. The selection of either the positive or negative slope is accomplished by gating circuits. Panel switch S903 provides a ZERO level input to IC101A. The ONE output of IC101A is applied to IC102B with the input signal. The inverted output is applied to IC102C, again inverted, and capacitively coupled to IC102D. Gate IC102D has a ONE level applied to both inputs from a voltage divider comprised of CR119–CR123 and R138/R139. The negative pulses applied to IC102D, pin 12, occur on the negative slope of the input signal. Gate IC102A is inhibited by a ZERO input from IC101F. A positive-slope selection applies a ONE level to IC101A that enables IC102A through inverter IC101F. Gate IC102B is inhibited by the ZERO output of IC101A. The output of IC102D is now a positive-slope signal in phase with the input signal. The output signal (CN) is applied to pin 24.

4.4.4 Clock Circuit Board.

Refer to Figure 6-5. The Clock Circuit board contains the clock oscillator, phase lock, and clock-selection logic.

Clock-Oscillator. The clock-oscillator circuit generates the 10-MHz time base for the instrument. Oscillator stability is achieved by means of a 10-MHz crystal in a proportional-controlled oven. The oscillator circuit is similar to the Butler oscillator, the crystal forming a feedback path between the emitters of a two-stage amplifier (Q601/Q602). The collector of Q601 is tuned to minimize amplifier phase shift. The circuit is designed so that Q602 is collector limited, ensuring a constant drive level to the crystal from the voltage divider, R608 and R609. A varicap (CR602) is connected in series with the crystal circuit and is biased by a dc voltage from the phase lock circuit. When an external reference signal is used to effect a phase-lock between the 10-MHz oscillator and the reference signal, this bias level is varied to tune the oscillator. The 10-MHz output at the collector of Q602 is coupled through C604 to the input of IC601A shaping circuit.

Clock Shaper and Decade Circuits. The output at pin 12 of the shaping circuit (IC601A) is a 10-MHz square wave driving a decade divider (IC602) that provides a 5-MHz output from pin 12 and a 1-MHz output from pin 11. The 1-MHz output drives a second decade (IC603) that divides the 1-MHz input down to a 100-kHz output at pin 11. The 5-MHz output of decade 1 is differentiated and then inverted by IC608A as the signal CA.

Phase Lock Circuits. The phase lock circuits develop a dc voltage proportional to the phase difference between the oscillator frequency and external reference frequency. The dc voltage is applied to a varicap (CR602) in the oscillator circuit to phase-lock the oscillator to the reference frequency.

Gates IC605C and IC605D apply the 1-MHz or 100-kHz clock signals, respectively, to the phase-detector, as selected by rear panel switch S906 (EXT STD FREQ). The external reference frequency is applied through pin 5 to the base of Q603 driver. The collector output of Q603 is applied to shaper circuit IC601B. The shaped output of IC601B is coupled through C608 to the Q604 base bias network, comprised of CR607, R618, R617 and C609, and causes Q604 to be turned off when a reference signal is present. The shaped output of IC601B is also coupled across C610 to IC604C. IC604C/D comprise a cross-coupled NAND gate flip-flop. The output of IC604D is turned on (ONE level) for a period of time proportional to the phase difference between the clock frequency and the external reference frequency; when the signals are in phase, the times on and off are equal.

The flip-flop output is applied to Q605 which turns on for each ONE level pulse output. When Q605 conducts, a ZERO level is applied to R620; when Q605 is off a +10-V level is applied. C621 charges to the average voltage at Q605 which is proportional to the phase difference between the clock and reference frequencies. This voltage is applied to varicap CR602 through isolating resistor R613. When no reference signal is present, both Q604 and Q605 will be saturated and the voltage on C621 will be determined by the voltage divider R619—R620.

Clock Selection Logic. Front-panel control S904 selects either the 1-MHz slow measuring rate or the 10-MHz fast measuring rate. The slow-rate signal, which is a ZERO level, is applied to pin 9 as signal $\overline{LG}$ ($\overline{SG}$ must be at the ONE level). A ZERO level at pin 9 is applied to IC605A and is also coupled to the J input of IC606A through a diode (CR610). NAND gate IC605A inverts the $\overline{LG}$ ZERO input to a ONE which enables the K input and allows the next CA pulse to set the flip-flop to the $\overline{Q}$ state. The $\overline{Q}$ ONE output is applied to IC607B. Gate signal G is also applied to the NAND gate as a ONE level when the count cycle starts, allowing 1-MHz clock pulses to be gated to IC604A. NAND gate IC604A inverts the clock pulses to output pin 12 as signal CT.

When S904 is placed in the FAST position a ZERO level is applied to pin 10 as the fast clock function gate $\overline{SG}$ ($\overline{LG}$ must be at the ONE level). The ZERO level is applied to IC605B and inverted to a ONE level output. The output of IC605B drives the J input of IC606A generating a ONE level Q output. The ONE output of IC606A enables IC607C and gates the 10-MHz clock pulses through IC607C to IC604A. The output of IC604A is now the fast 10-MHz clock signal.

When S904 is placed in the AUTOMATIC position, the signals $\overline{SG}$ and $\overline{LG}$ are both a ONE level. NAND gates IC608B and IC604B now control the fast or slow clock functions; IC608B receives inputs from the time register and IC604B receives an input from Period Register 4 and the gate signal.G. The clock speed is selected according to the frequency of the signal being measured. The switchover points are 6-Hz for decreasing frequency and 8-Hz for increasing frequency. The Time and Period Registers are reset to the $\overline{Q}$ state which initially applies Zero levels to IC608B and IC604B; signal G to IC604B is a ONE. The inverted ONE outputs are applied to IC605A/B, which apply a ZERO level to the J and K inputs of IC606A. If the time register overflows, IC608B generates a time overflow signal ($\overline{TOF}$) at pin 23 and applies a ZERO level to IC605A. The output of IC605A goes to a one level that enables the K input of IC606A. The next CA(5-MHz) clock pulse sets the flip-flop to the $\overline{Q}$ state, enabling IC607B and gates the 1-MHz clock signal (CT) to pin 12 via IC604A.

If the Period Register generates signal NQ4 (pin 11) the output of IC604B drops to a ZERO level that is applied to IC605B, which generates a ONE level to enable the J input of IC606A. The next CA clock pulse sets the flip-flop to the Q state, applying a ONE level to IC607C, gating the 10-MHz clock signal (CT) to pin 12 via IC604A.

Gate IC607A receives the normally ONE level reset signal ($\overline{RM}$) from pin 14. The other two inputs are normally at a ONE level, being tied to a positive voltage divider. When IC606A changes state either the Q or $\overline{Q}$ side will drop to a ZERO level. A negative pulse is coupled across C613 or C614 to one input of IC607A. Gate IC607A generates a ONE level output that is applied to the J input of IC606B. A ZERO level at $\overline{RM}$ will also cause a ONE level at IC607A. When the J input is enabled, the next CA clock pulse sets the flip-flop to the Q state. The $\overline{Q}$ side drops to a ZERO level, generating the abort signal ($\overline{ABT}$). The abort signal ($\overline{ABT}$) is applied to circuits that generate resets RA and RC. Flip-flop IC606B is reset at the end of the display time when the K input is energized by signal DTA. The instrument then commences another count at the proper clock speed that has been selected by IC606A.

4.4.5 Gate Circuit Board.

See Figure 6-7. The Gate Circuit board contains the stop logic, gate enabling, display time, and program misfunction detecting circuitry.

Stop Logic. The stop logic gates receive inputs from the time register (TQ16—TQ20) and from the period register (NQ1, $\overline{NQ1}$, NQ2). A cross-coupled NAND gate flip-flop (IC156C/D) is reset at the end of the compute cycle by signal $\overline{RA}$ from pin 8 and applies at ONE output to IC154D, IC153B, IC153A and a ZERO to IC154C.

When the inputs NQ1 and NQ2 (pins 4 and 10) are both ZERO levels the flip-flop remains set, applying a ONE to GATE IC153A. The ZERO level NQ2 signal is inverted by IC155F and applied to IC153A as a ONE. The ONE level signal $\overline{NQ1}$ (NQ1 = ZERO) enables IC153A and generates a ZERO output to the hard-wired OR gate (the input to

IC155C). The OR gate output is inverted by IC155C and applied to IC153C. When TQ19 and TQ20 reach a ONE state the ZERO output of IC153C sets the stop flip-flop (IC158A/B). For the 10-MHz clock, this occurs 78.6432-ms after the gate is enabled. Gate IC158A applies a ONE output to the K enabling gate of flip-flop IC157. If NQ1 is a ONE and NQ2 a ZERO, gate IC153B is enabled. Now TQ18, TQ19 and TQ20 are required to stop the count, corresponding to a time of 91.7504-ms.

If NQ1 is a ZERO and NQ2 is a ONE, gate IC154D is enabled, requiring TQ17—TQ20 to stop the count, which corresponds to a time of 98.3040-ms. If NQ1 is a ONE and NQ2 is a ONE, IC156B is enabled, generating a ZERO output which sets (IC156C/D). The ONE output of IC156C now enables IC154C, requiring TQ16—TQ20 to stop the count, which corresponds to a time of 101.5808-ms.

Control Gates. When the stop flip-flop (IC158A/B) is set, enabling the K gate of flip-flop IC157, the next count input (CN) resets IC157 to the $\overline{Q}$ state. The Q ZERO output is applied to pin 7 as the Time Register clock gate signal (G) inhibiting the clock signal (CT). It is also applied to IC158D, inhibiting the gated count signal (CNG). The Q ZERO output of IC157 is inverted by IC155A and applied to IC152A with the normally ONE level input from pin 23 ($\overline{ABT}$). The ZERO output of IC152A is inverted by IC155B which generates a ONE level signal ($\overline{G}$) at pin 21. The signal $\overline{G}$ is delayed approximately 3-μs by C151 to allow carry propagation in the ripple counters before the computation period. The ONE level $\overline{G}$ signal is also applied to IC152D with the ONE output of stop logic flip-flop gate IC158A, generating a ZERO level output that is inverted by IC152C and applied to pin 22 as the $\overline{GC}$ signal. The $\overline{GC}$ ONE level signal is applied to the Time and Period Counter Registers as shift inputs to enable computation.

Display Time Circuits. At the end of the computation period the reset A ($\overline{RA}$) signal is applied to IC151D of the display-time NAND gate flip-flop (IC151C/D), generating a ZERO level from IC151C. The gate output is applied to the emitter of Q153 and to R158, in the display time control circuit. An external 0-to-100-kΩ potentiometer (R902) on the front panel (DISPLAY TIME) is connected in parallel with R158. Q153 is normally cut off by a ZERO level signal at the base from IC152B. DISPLAY TIME potentiometer R902, R158, R151 and C152, comprise the timing circuit. The voltage across C152 is applied to the emitter of Q152. When the display time gate (DTA) drops to a ZERO level at reset A ($\overline{RA}$) time, the voltage across C152 decays exponentially with a time constant (RC time) determined by the DISPLAY TIME potentiometer. When the voltage across C152 decays to a level determined by voltage divider (R155, R152, R156) Q152 begins to conduct, turning on the complementary latch circuit Q151/Q152. This causes C152 to recharge and turns on Q154, applying a ZERO level to the display time flip-flop (IC151C/D) and resetting the flip-flop (IC151C/D) to a ONE level. The ZERO output of Q154 also sets the NAND gate flip-flop (IC151A/B), which generates a ONE level output from IC151B that is applied to the J enabling gate of flip-flop IC157. The next CN clock pulse sets IC157 to the Q state, causing the (G) gate signal to rise to a ONE level, gating on the clock count to the Time Registers and gating the count (CN) clock signal to the Period Register. The signals G and GC now drop to a ZERO level during the counting period. The ZERO level output to IC157 resets the flip-flop (IC157A, IC151B), causing signal STG to return to a ONE level, and the gate flip-flop is inhibited until the next RA signal generates a subsequent dispaly time.

Program Misfunction Detection. Gates IC156A and IC159A—D form a circuit to detect and correct certain abnormal conditions that can occur when power is first applied to the instrument. Gates IC159A, B, and D have their outputs connected in the hard-wired OR configuration to the input of IC159C. Thus, if any of the three has a ZERO output, the output of IC159C is at the ONE level. If all three have a ONE level output, then, after being delayed for 1.5-ms by C154, the output is at the ZERO level. This ZERO level output is applied to the manual reset ($\overline{RM}$) circuit to establish normal operation.

Gates IC159A, B, and D will have ONE level outputs when one each of their inputs is at the ZERO level.

The $\overline{K}$ signal is derived from the Add Cycle and Reset Board and is at the ZERO level during the computation cycle. It is applied to one input each of IC159A, B, and D. Thus, if the time for computation exceeds the 1.5-ms delay, the instrument will reset.

Gate IC159A receives its other input from IC156A, whose two inputs are $\overline{PC}$ and DTA. $\overline{PC}$ (print command) is at the ONE level during printout, DTA is at the ONE level except during the display cycle. When both $\overline{PC}$ and DTA are at the ONE level, IC156A will apply a ZERO level to IC159A.

Gate IC159B receives its other input from the Q output of gate flip-flop IC157 (G), which is a ONE level during the count cycle and a ZERO level during the compute cycle.

Gate IC159D receives its other input from IC151A/B (STG), which is at the ZERO level except from the end of the display cycle to the opening of the gate.

This combination of conditions (DTA, $\overline{PC}$ = ONE; STG, G = ZERO) normally occurs only during the computation cycle. If it persists beyond the 1.5-ms delay, the instrument is reset.

4.4.6 Shift/Count Register Circuit Board.

See Figure 6-8. The Shift/Count Register Circuit board contains 12 AND/OR input J-K flip-flops. The register is used in both the Time and Period Accumulator Registers and functions as a ripple counter for accumulating counts and as a shift register for arithmetic computation.

Refer to IC201. IC pins 1 and 12 are tied together and receive the input clock signal (count or time) from

pin 2. IC pin 13 is connected to a ONE level and the enabling gate (GC) is at a ONE level during the count cycle. This method of connection allows the counter to operate as a toggle J-K flip-flop. The flip-flop changes state with each positive input pulse. The rise of the pulse enables the input gates and the fall of the pulse sets the Q and $\overline{Q}$ outputs. Each succeeding stage is capacitively coupled to the following stage. A propagation time is required for carriers because of the ripple effect.

A preset input sets all stages to the Q state at reset time A. The output signals (Q1 through Q12) are complementary to the IC outputs. This provides a forward counter where the Q outputs are all ZERO when the register is preset.

When the input count is stopped (GC at ZERO level), the toggle input gates are disabled. Shift pulses (CS) are applied to the J and K gates and the accumulated count is shifted from the most significant end of the register out of the input (Q1, $\overline{Q1}$) stage for computation in the Arithmetic Section.

The Time and Period Registers each consist of two register boards for a total of 24 stages each.

4.4.7 Arithmetic Program Circuit Board.

See Figure 6-9. The Arithmetic Program Cycle board contains the arithmetic program cycle circuits, the full adder, and the multiply-by-10 circuit.

Program Cycle Circuit. The arithmetic process consists of subtract, add and multiply functions. These functions are gated by the outputs of IC408A and IC407A/B. Flip-flop IC406A is preset to the Q state by the $\overline{RA}$ signal and the Q output is applied to the J input of IC408A (which provides the subtract enable gate to the adder circuit) and to gate IC405A. When the compute cycle commences, the first CP pulse resets IC406A to the $\overline{Q}$ state, and sets IC408A to the Q state, enabling the subtract function at the adder input. The same CP pulse applied to gate IC405A sets the carry storage flip-flop IC406B to the ONE level and generates the $\overline{CD}$ pulse for the Quotient Registers. The Q output of IC406B is applied as one of the enabling inputs to IC410A. The Q output of IC408A is applied to IC410C; the other input is the $\overline{CARRY}$ output from the adder. If there is no carry, the output enables the J input of IC407B. The next CP pulse sets IC407B to the Q state and IC408A to the $\overline{Q}$ state. This disables the subtract function and enables the add function to the adder input.

When the add cycle is complete the next CP pulse sets IC407A to the Q state and IC407B to the $\overline{Q}$ state. The add function is disabled and the multiply function is enabled at the adder input. The next CP pulse resets IC407A to the $\overline{Q}$ state and sets IC406A to the Q state. The Q output of ONE from IC406A enables the J input to IC408A, readying the program cycle shift counter for another cycle.

Multiply-by-10 Circuit. The multiply-by-10 circuit consists of three shift counter stages following the Period Register. The first Period Register stage output (NQ1, $\overline{NQ1}$) is applied from pins 3 and 21 to the J and K inputs of IC409A and is shifted through IC409B and IC408B by the shift pulses (CS). This in effect multiplies the quantity in the period register by 2, 4, and 8 progressively. The quantity multiplied by 2 is applied to one adder input and the quantity multiplied by 8 is applied to the other:

Example

$$(2 \cdot 2) + (2 \cdot 8) = 20 = (2 \cdot 10)$$

Adder Circuits. AND/NOR gate IC404 is the addend input circuit for the adder and AND/NOR gate IC401 is the augend input circuit. The enabling subtract gate from IC408A is applied to the addend input with the complement of the time register ($\overline{TQ1}$). The subtract gate is applied to the augend input with the period register output (NQ1).

The add gate from IC407B is applied to the addend input with TQ1 and to the augend input with NQ1. The multiply gate from IC407A is applied to the addend input with the output of IC409A ($\overline{NQ1} \cdot 2$). The result is applied to the augend input with the output of IC408B (NQ1 · 8).

The addend and augend outputs are applied to a full adder (IC402 and IC403). The sum output of IC402 is applied to pin 9 as the SUM (Σ) and through inverter IC405C as the complement ($\overline{\Sigma}$). The carry output of IC403 is stored in IC406B. The Q output of IC406B is applied to IC410A that is enabled only during the subtract operation. The output of IC410A is the signal CF, which drives the Quotient Registers and is clocked at the CP pulse rate. The carry complement ($\overline{Q}$) output of IC406B is applied to the adder as the carry-in for the next operation.

4.4.8 Quotient Register A Circuit Board.

See Figure 6-10. The Quotient Register A board contains gating circuits and decade counters for the three most significant digits.

The most significant decade counter unit (DCU) is IC253. All the DCU's are reset to ZEROES by the reset C (RC) pulse at the beginning of the computation cycle.

The 1-2-4-8 BCD outputs of IC253 are ZEROES and are applied to inverters IC259C–F, which generate the BCD output signals 1F$\overline{A}$ (1), 1F$\overline{B}$ (2), 1F$\overline{C}$ (4) and 1F$\overline{D}$ (8). The ONE level signals are applied to IC257B, which generates a ZERO output that inhibits the J input IC254A. The reset C ($\overline{RC}$) signal is also applied to the clear inputs of IC254A/B, and to the NAND gate flip-flop (IC256B/C). The ZERO level $\overline{RC}$ signal sets the output of IC256C to a ONE level that enables IC256D. The carry signal (CF) from the Arithmetic Program card at pin 22 is applied to IC256D. The output of IC256D is applied to IC256A, which generates the count signal for the DCU. The output of IC256A is

normally ZERO and goes to a ONE level whenever a CF pulse is generated or a carry is received from the next less significant DCU.

Flip-flop gate IC256B generates a ZERO output at reset time C ($\overline{RC}$) that is inverted by IC257A and applied to the J input of IC254A. This J input is, however, still inhibited by the ZERO output of IC257B. The first CF count to the DCU (and any subsequent count) applies one or more ZEROES to gate IC257B, generating a ONE output. The J input of IC254A is now enabled.

After the Arithmetic Program cycle loads the first (most-significant) DCU, the signal CD is generated and applied to IC254A, setting it to the Q state; the $\overline{Q}$ output drops to a ZERO level and resets the output of flip-flop gate IC256B to a ONE level. The ONE level is inverted by IC257A and applied as an inhibiting level to the J input of IC254A, which remains in the $\overline{Q}$ state for the remainder of the display cycle. Gate IC256D is inhibited by the ZERO output of IC256C; therefore, the only input to the DCU (IC253) is from a preceding-stage carry. IC254A now enables IC255D, which allows signal CF to load the next less significant DCU (IC252). The Q output of IC254A also enables the J input of IC254B. At the end of the second Arithmetic Program cycle, signal CD flips IC254B to the Q state, enabling the CF input to the third DCU (IC251). The Q output of IC254B (ONE level) is applied to pin 23 as signal (QA), which enables the J input to the gate flip-flop for the fourth DCU on Quotient Register B board. The signal 4FD is received from the fourth DCU on Quotient Register B board as the carry input to the third DCU (IC251).

4.4.9 Quotient Register B Circuit Board.

See Figure 6-10. Quotient Register B contains the decade counter units (DCU's) and associated gates for the fourth, fifth and sixth (least significant) digits. Each DCU is enabled by a gate flip-flop that is enabled by the Q output of the preceding (more-significant) DCU gate flip-flop. Signal QA from the Quotient A Register board is applied to pin 23 as the enabling J input to IC301A. Refer to paragraph 4.4.8 for the operational theory of the DCU gating. The fourth, fifth and sixth decades are loaded and generate carries in the same manner as the second and third DCU's on Quotient Register A. The sixth DCU receives a round-off carry (when required) from a divide-by-five counter (IC309) as the last cycle of the arithmetic program. Flip-flop IC308B generates the signal QC which is applied to the Add Cycle and Reset Board.

4.4.10 Add Cycle and Reset Board.

See Figure 6-11. The Add Cycle and Reset board contains the reset A generator, reset C generator, shift pulse and add cycle pulse circuits. It also contains the print-command circuits.

Arithmetic Program Cycle Counter. The program cycle pulse (CP) at pin 20 is generated by the divide-by-32 counter and its associated gates. The counter is basically comprised of flip-flop stages IC456, IC458A/B IC460A/B. The clock input is a 5-MHz signal (CA) from the clock circuit board. The enabling gate for the counter is IC455D. The enabling gate receives the gate signal (DC) from the arithmetic program board and signal (QC) from the Quotient B board.

Either DC or QC is at a ZERO level during the compute cycle. Either ZERO level input to IC455D generates a ONE output that enables IC456. The five counter stages are preset to the Q state by the RA reset signal. The shift pulses (CS) at pin 7 are generated from IC455B by the 5-MHz clock signal CA and a gate signal from the divide-by-32 counter.

The gate signal is generated by IC455C when the Q outputs of IC460A or IC460B are a ZERO level. The two flip-flop Q outputs are not a ZERO until after the second clock count. At the third clock count the Q outputs of IC460A/B are a ZERO and remain so until after clock time 26 when they are both a ONE level. A total of 24 shift pulses ($\overline{CS}$) are generated, corresponding to the number of stages in the Time and Period Registers. The shift-pulse gate signal is also applied to pin 24 as the signal GCS that generates the CS shift-pulse signal on the Arithmetic Program board. At clock time 31 the arithmetic-cycle pulse CP is generated by the AND/NOR gate circuit (IC461) and applied to pin 20.

A second CP pulse is generated at the beginning of the next cycle whenever $\overline{DC}$ is at the ZERO level.

When the round-off stage in the Quotient B Register is enabled the signal QC at pin 17 rises to a ONE level. When the Arithmetic Cycle Generator completes the last sequence, the signal DC at pin 15 rises to a positive level. NAND gate IC455D now generates a ZERO output and inhibits the divide-by-32 counter.

Reset Circuits. The reset A flip-flop (IC454) is normally reset to the $\overline{Q}$ state by the CA 5-MHz clock input. During the compute cycle the output of IC455A is a ZERO level, setting the output of NAND gate flip-flop stage IC453A to a ONE. The outputs of IC455A and IC453A are applied to the J enabling gate of IC454, which is inhibited during the compute cycle.

At the end of the compute cycle, signals DC and QC rise to a ONE level and the output of IC455A goes to a ONE level. The J enabling gate of IC454 is now enabled. The next CA clock pulse sets IC454 to the Q state, generating the reset A (RA) signal at pin 13. The $\overline{Q}$ ZERO level output is applied to IC453A/D producing a ZERO level from IC453A and a ONE level from IC453D, enabling the K input of IC454. The next CA pulse resets the flip-flop to the $\overline{Q}$ state, terminating the RA signal. The ONE level Q output is also applied to IC457A to generate the signal $\overline{RA}$, which presets the divide-by-32 counter stages to the Q state, ready

for the next compute cycle. Signal $\overline{ABT}$, (pin 16) is a negative pulse generated by manual reset or an automatic change in clock speed. The negative pulse is coupled across C451 and applied to the preset input of IC454 to generate signal RA.

Flip-flop IC452 is the reset C generator and is normally set to the $\overline{Q}$ state by the CA clock pulses. The signal $\overline{G}$ is at a low level during the count cycle and is applied to IC453B, setting the output to a ONE level. Signal $\overline{G}$ and the ONE output of that gate are applied to the J enabling gate of IC452. When $\overline{G}$ rises to a ONE level (end of count cycle) the J gate of IC452 is enabled, allowing the next CA clock pulse to set the flip-flop to the Q state. A ONE level Q output generates the reset C (RC) signal at pin 8. The next CA clock pulse resets IC452 to the $\overline{Q}$ state.

Print Command Circuit. The reset A signal (RA) is applied to a cross-coupled NAND gate flip-flop (IC451C/D) through inverter IC457B. The ZERO level input to IC451D sets the output of IC451C to a ZERO, generating the print command PC at pin 18. If pin 21 (PCT) has no connection, the flip-flop will remain with a $\overline{PC}$ ZERO signal out for a period of time determined by C453, R454 and the output of IC451A. After an RC time delay, the output of Q451, inverted to a ZERO level by IC451A, resets the flip-flop.

4.4.11 Range Counter Circuit Board.

See Figure 6-12. The Range Counter Circuit board contains the prescaler gating circuits, range counter and lamp driver circuits.

Prescaler. The prescaler circuits are controlled by panel switch S907. The three scaling factors are 1, 10 and 100. The prescaler circuits control the readout dimensions to furnish a direct reading when the instrument is preceded by a 10:1 or 100:1 scaler. For a prescaler switch setting of 1X, the 10X and 100X inputs at pins 5 and 3, respectively, will be a ONE level. The 10MG signal (pin 9) is at a ONE level when the 10-MHz fast clock speed is used, and at a ZERO level when the 1-MHz low clock speed is used. NAND gates IC351A/B/F control the output levels of three hard-wired OR gates (IC352C–351E, IC352A–352B, and IC352D–353D). The OR gate outputs control the state of the first three range-counter flip-flops (IC356A/B and IC357A). The fourth flip-flop (IC357B) is always reset to the $\overline{Q}$ state by the $\overline{RC}$ signal from IC354B. Flip-flops IC356B, 356A and 357A are either preset or cleared in various combinations according to the prescaler factor selected and the high-speed clock gate (10MG) as indicated in Table 4-1. The clock pulses for the first two flip-flops are the CD pulses occurring at an asynchronous rate whenever pulse CP and a completion of an arithmetic cycle occur simultaneously. The following two flip-flops are clocked by the Q output of IC356A. The flip-flop coutputs are applied to the lamp-driver gates.

Lamp Drivers and Gates. The lamp-driver gates for the decimal-point indicators are IC358D (DP3), IC359D (DP4) and IC359E (DP5). The gates are enabled in the appropriate sequence by the range-counter flip-flops. When a gate is enabled it generates a ZERO level output that is applied to its respective lamp-driver emitter. The lamp driver conducts, enabling that particular neon-indicator lamp.

The lamp-driver gates for the range indicators are IC358C, IC359F and IC359C. They are gated by the outputs of IC357A/B and operate in the same manner as the decimal-point circuits, enabling an associated lamp driver.

Low Frequency Circuit. The LOW FREQUENCY indicator lamp is energized when the input frequency is too low for operation on the appropriate range (high or low).

Q357 generates the signal LFI at pin 18 that drives the indicator lamp. A cross-coupled NAND gate (IC360A/D) enables Q357 if the signal $\overline{TOF}$ is generated during the count cycle. Signal $\overline{G}$ (pin 11), which is low during the count cycle, is applied to IC355A, inverted, and applied as a ONE level to IC358B. Signal $\overline{TOF}$ is generated as a ZERO level whenever a Time Register overflow occurs. Gate IC358A receives $\overline{TOF}$ from pin 20, inverts it, and applies a ONE level to the other input of IC358B. Gate IC358B generates a ZERO output which is applied to pin 6 as the reset ($\overline{RM}$). The ZERO output also sets the flip-flop to a ZERO output from IC360A. Lamp-driver Q357 conducts and lights the LOW FREQUENCY indicator lamp. The

TABLE 4-1

PRESET COMBINATIONS FOR RANGE COUNTER FLIP-FLOPS

Range	Fast	Slow	IC356B	IC356A	IC357A
PRESCALER		x100	1	0	0
	x100	x10	0	1	0
FACTOR	x10	x1	0	0	1
	x1		1	0	1

indicator lamp will remain lighted until reset C (RC) occurs at the end of the next complete count cycle, or until the no signal circuit is enabled.

If the FAST-SLOW switch is turned to the SLOW position and the lamp is lighted, it will remain lighted until the end of the next count cycle when reset C (RC) will be generated to reset the flip-flop. The signal RC is applied to IC360A via pin 14.

No Signal Circuit. A front-panel indicator (NO SIGNAL) will energize after a delay of approximately 1.7 s (1 instrument cycle) if there is no count signal present at the input. The signal NSI (pin 21) is generated by Q358. A cross-coupled NAND gate flip-flop enables Q358 whenever signal $\overline{STG}$ (pin 24) remains at a ZERO level for more than approximately 1.7 s. Signal $\overline{STG}$ is normally a ONE level and drops to ZERO upon completion of display time for approximately one count period or less. If a count input is not received, $\overline{STG}$ remains at a ZERO level. When $\overline{STG}$ is a ONE, IC359B applies a ZERO to IC360C and IC359A applies a ZERO through a time-constant network to the base of Q359; the ZERO level inhibits Q359, which applies a ONE to IC360B. Gate IC360C applies a ONE to lamp driver Q358 to inhibit the indicator lamp. When $\overline{STG}$ drops to a ZERO level, IC359B applies a ONE to IC360C. IC359A applies a ONE to Q359 via the RC time-delay network (CR353, CR354, CR355, CR359, R361, R353 and C352). There is a time delay (approximately 1.7 s) slightly longer in duration that one instrument cycle. If $\overline{STG}$ does not return to a ONE level within this time, the delayed ONE causes Q359 to conduct and sets the flip-flop output gate (IC360C) to a ZERO, enabling the lamp driver and resetting the Low Frequency flip-flop (IC360A/D) through diode CR352.

4.4.12 Buffer Circuit Board.

See Figure 6-13. The Buffer Circuit board is mounted on the underside of the instrument chassis and is not a plug-in board. It contains five IC units, each consisting of 6 NAND-gate buffer inverters. The buffers provide an interface for instrument display information and the SO904 DATA OUTPUT plug. The Buffer Circuit board is mounted by screws to the chassis and is hard-wired.

4.4.13 Readout Circuit Board.

See Figure 6-10. The Readout Circuit board contains the anode power supply for the readout indicators, IC BCD/decimal decoders for the readout indicators, a control switch to disable the anode voltage for the compute operation, and the indicator lamps and hardware.

The Readout Circuit board is mounted to the chassis and is hard-wired. Only the neon indicator lamps are removable plug-ins.

A power supply rectifier/filter assembly receives 212-V ac from power transformer (T501) that is applied to terminals AT731 and AT732. A bridge rectifier (CR707–CR710) and filter (R731, C701, C702 and bleeder) provide approximately 250-V dc to the anodes of the neon indicator lamps. The negative side of the supply is referenced to chassis ground through diode CR711, and is therefore one diode drop (about 0.6 V) above ground.

A switching stage (Q701) receives the signal $\overline{GC}$ from the gate circuit board. The emitter of Q701 is tied to the negative return and the collector to the anodes of each neon indicator through coupling diodes. When $\overline{GC}$ is at a ONE level during the compute cycle, Q701 conducts, lowering the anode voltage. Limiting resistors (R701 through R706) establish the proper current in each tube. During the count cycle, $\overline{GC}$ drops to a ZERO level, causing Q701 to turn off, unloading the anodes. The neon indicators now display the previously computed count.

Six decoder/drivers (IC701 through IC706) receive BCD inputs from the Quotient A and B Register boards. The BCD data is converted to decimal information that drives the neon indicator lamps.

Service and Maintenance—Section 5

5.1 SERVICE.

The two-year warranty attests the quality of materials and workmanship in our products. When difficulties do occur, our service engineers will assist in any way possible. If the difficulty cannot be eliminated by use of the following service instructions, please write or phone our Service Department (see back of manual), giving full information of the trouble and of steps taken to remedy it. Be sure to mention the serial and type numbers of the instrument.

5.2 INSTRUMENT RETURN.

Before returning an instrument to General Radio for service, please write to our Service Department or nearest District Office requesting a "Returned Material Tag." Use of this tag will ensure proper handling and identification. For instruments not covered by the warranty, a purchase order should be forwarded to avoid unnecessary delay.

5.3 MINIMUM PERFORMANCE STANDARDS.

Perform all the steps listed in paragraph 3.3 to establish that the 1159 meets minimum performance standards.

The following additional tests may be performed if required.

5.3.1 Input Sensitivity.

This test applies a sinewave input signal from a calibrated source to the instrument input circuits. Observe the counter-display indicators for a steady, accurate indication.

a. Connect the test oscillator with a calibrated voltage output to J901 INPUT jack. Match the test-oscillator output impedance to the instrument input impedance (see specifications) for accurate voltage readings.

b. Adjust the oscillator frequency for an output of 2-MHz at approximately 15-mV rms output level.

c. Adjust TRIG LEVEL control for a stable reading on the display indicators.

d. Reduce the output voltage of the test oscillator while adjusting the TRIG LEVEL control for a stable reading until the display indicators show a continuously erratic reading.

e. Increase the output level of the test oscillator until a stable reading is obtained. The test oscillator output voltage level should read 10-mV rms maximum.

NOTE

Continue the procedure up to 10-MHz at desired frequency increments. It will be necessary to switch to a high frequency test oscillator to cover the instrument frequency range.

At frequencies from 10-MHz to 20-MHz the voltage level reading should be 20 mV rms maximum.

5.3.2 Bandwidth.

The bandwidth test consists of measuring the −3dB points (sensitivity) at each bandswitch position (1 kHz, 10 kHz, 100 kHz, 1 MHz and 10 MHz).

The following procedure is applied to a bandwidth measurement at 1 kHz. The same procedure is applied to all other bandswitch frequency positions with due consideration to the frequency range involved.

a. Connect a test oscillator with a variable calibrated output control and a frequency range of 0.5 kHz to 20 MHz to the INPUT jack (J901/J902).

b. Place the INPUT BAND switch on the 1159 to the 1 kHz position.

c. Adjust the test oscillator frequency to 0.8 kHz and make a sensitivity check as described in paragraph 5.3.1. Record the voltage (1-mV rms or less).

d. Increase the oscillator frequency toward 1 kHz, adjusting the oscillator and counter controls until the display indicators are just stable.

e. When a frequency is reached where the test-oscillator output voltage is 1.413 times the voltage recorded in step c, observe the test oscillator frequency. It should read 1 kHz. This is the −3dB cutoff point for high-frequency noise.

NOTE

Repeat this procedure at each remaining frequency position of the INPUT BAND switch.

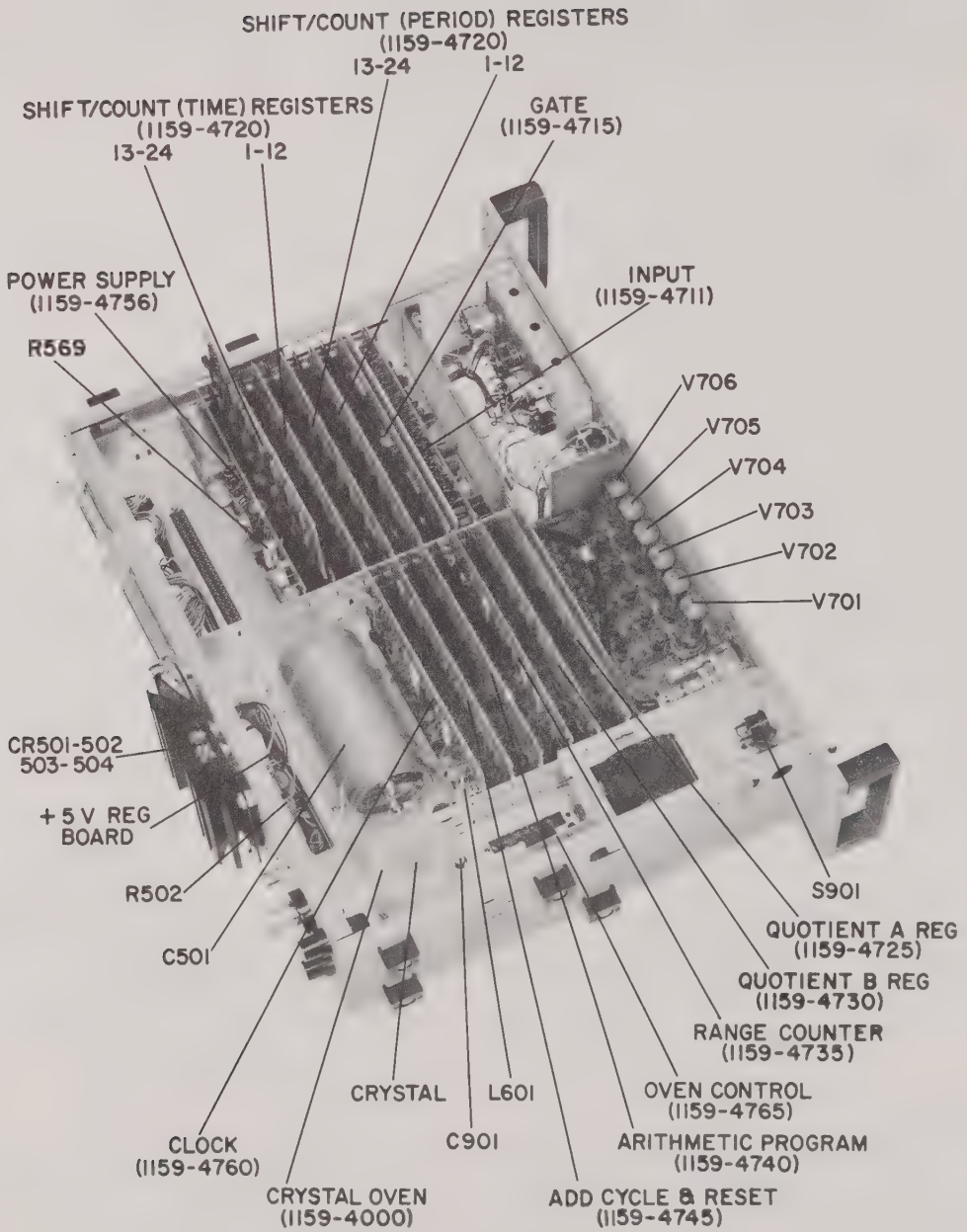


Figure 5-1. Component accessibility — top view showing the Time Register (13–24) etched-circuit board in its service position, connected through the extender board.

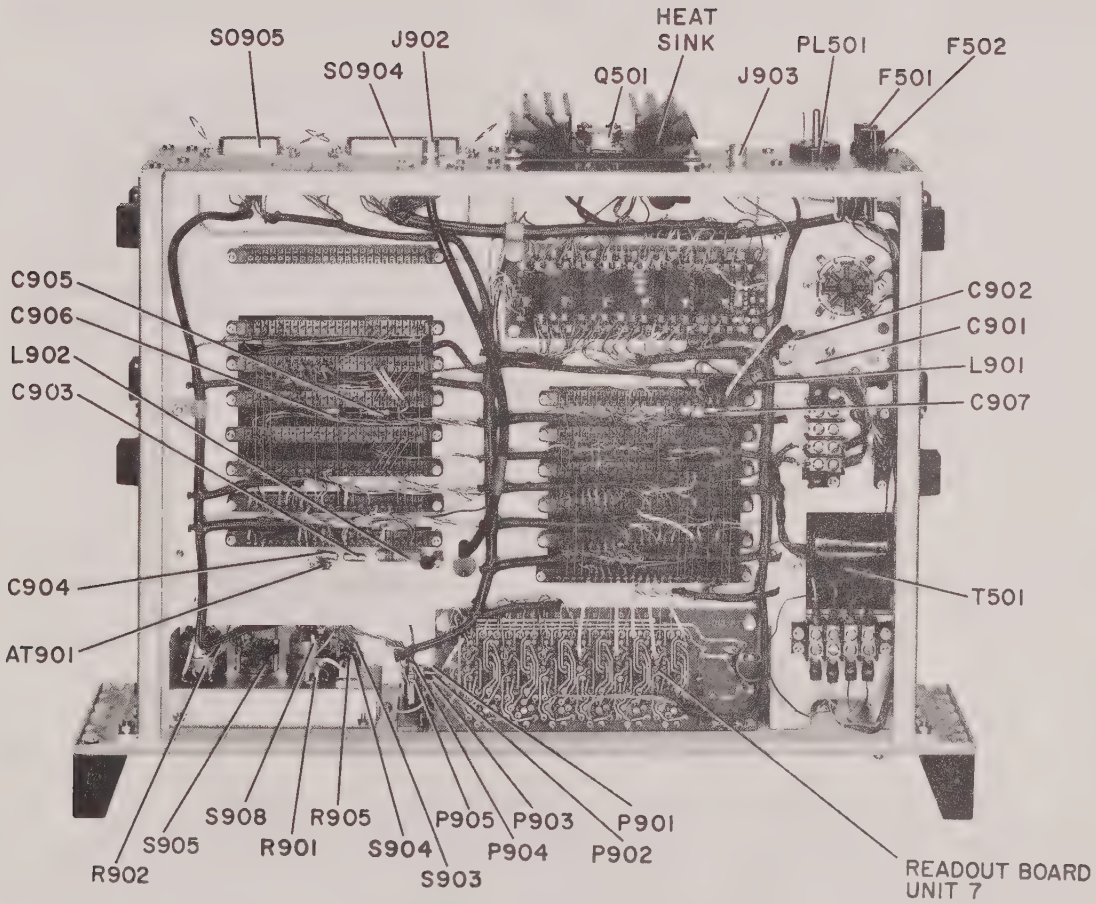


Figure 5-2. Component accessibility — bottom.

5.4 COMPONENT ACCESSIBILITY.

Figures 5-1 and 5-2 identify the components of the 1159 with their corresponding locations.

5.5 MAINTENANCE.

The 1159 counter features modular construction that simplifies troubleshooting and repair. The instrument is completely solid-state circuitry comprised, for the most part, of integrated circuits. A minimum of discrete components supplement the integrated circuits.

The instrument has only 3 basic calibrating adjustments; clock oscillator, power supply, and trigger-level zero. Once these adjustments are made, routine periodic adjustments are not required.

5.5.1 Etched-Board Maintenance.

The etched boards can be raised (by means of the extender board located in SO903) above the instrument to enable easy access to components and test points.

The 24-pin extender board (P/N 4215-2034) accommodates all the plug-in boards except the oven control board (P/N 1159-4765). The etched-circuit boards are constructed with the pin-base off-center so they cannot be reversed in the sockets and damage components.

CAUTION

The etched boards can be reversed when plugged into the extender board. Extreme care must be taken to ensure that the boards are plugged into the extender board with the circuit components facing the rear of the instrument. Circuit boards can also be inserted into the wrong sockets. Particular care must be taken not to inadvertently interchange boards. Refer to Table 5-1 for board location and corresponding socket.

Defective boards may be repaired locally or sent to the nearest General Radio Repair Center for repair or replacement.

5.5.2 Module Repair and Replacement.

The etched-circuit boards listed in Table 5-1 are easily removed for repair and replacement. Troubleshooting is accomplished by signal analysis as covered in paragraph 5.6. A single integrated circuit (IC) component may have units in several different circuits. It is not practical to test each complete IC for a good-bad condition for this reason. Circuit boards, in general, may not be interchanged except for the four 4720 shift-register boards. The 4720 boards

Table 5-1
ETCHED-CIRCUIT BOARDS AND MODULES
(See Figure 5-1)

Qty	GR Part No.	Socket No.	Circuit Function
1	1159-4765	SO901	Oven Control
1	1159-4000	SO902	Crystal Oven
1	4215-2034	SO903	Extender Board
1	1159-4711	SO910	Input
1	1159-4715	SO915	Gate
4	1159-4720	SO921	Period Register 1–12
		SO922	Period Register 13–24
		SO923	Time Register 1–12
		SO924	Time Register 13–24
1	1159-4725	SO925	Quotient A
1	1159-4730	SO930	Quotient B
1	1159-4735	SO935	Range Counter
1	1159-4740	SO940	Arithmetic Program
1	1159-4745	SO945	Add Cycle and Reset
1	1159-4760	SO960	Clock
1	1159-4755	SO502	+ and −15 V Supply
1	1159-2790	non plug-in	Mounted beneath chassis
1	1159-2771	non plug-in	Mounted on chassis
1	1159-2781	non plug-in	Mounted on rear of chassis

may be interchanged to confirm a trouble-anaylsis location. All four boards, however, are required to be in proper working order for normal operation of the instrument.

Crystal Oven. The crystal oven is an octal plug-in that is located in SO902. The crystal is accessible by removal of the oven cover. The oven heater and thermistor are a potted assembly and cannot be repaired. If there is an oven failure a new oven assembly must be ordered.

Power Transformer T501. The left side of the instrument chassis must be removed whenever T501 is replaced, as there is insufficient clearance to remove the transformer from the chassis.

5.6 TROUBLE ANALYSIS.

5.6.1 Introduction.

Due to the relatively complex program of the 1159 it is impractical to evolve a go, no-go, troubleshooting procedure as is possible with a simple series device. Trouble analysis consists of signal tracing in the most logical manner.

When a trouble symptom appears it is recommended that a complete operational checkout be performed prior to troubleshooting. (See Section 3- Operation). This will, in many cases, isolate the trouble to a section of the instrument.

When troubleshooting, check all panel controls for proper function and signal levels as well as the internal circuitry.

The following trouble analysis steps will assist in localizing failure to a specific module, and in most cases to a specific module area or component. Defective boards may be repaired locally or sent to the nearest General Radio Repair Center for repair or replacement.

When a particular module or component is indicated as defective, it is recommended that the socket or wiring connections be checked for proper indications prior to repair or replacement. Dirty socket connections, pin misalignments and improper seating are often a source of troubles. It is also recommended that a thorough visual inspection be made to locate any unintentional shorts or grounds. Connector pins are easily bent by test probes and accidental contact with tools. A magnifying glass will prove invaluable for locating bent or touching pins on circuit board sockets.

NOTE

When the trouble symptom has been localized to an etched-circuit board, it is recommended that the first step be to check all dc voltage inputs for proper level with respect to chassis ground before proceeding to isolate the defective component. This step is assumed in the following trouble analysis procedure and will not be repeated.

It is necessary to have a thorough understanding of operational theory to be able to effectively troubleshoot the complex program of the 1159 instrument.

NOTE

The trouble analysis steps refer to signals that are illustrated in Figures 6-2A and 6-2B. Figure 6-2C is a simplified overall logic diagram containing key signals and may be used to isolate troubles to functional sections.

5.6.2 Test Equipment Required.

The specifications listed in Table 5-2 are those necessary for troubleshooting or calibrating the 1159 and are not necessarily those of the suggested equipment.

Table 5-2
LIST OF TEST EQUIPMENT

Function	Recommended Type or Model *	Minimum Performance Characteristics
Voltmeter ac–dc	GR 1806	Dc impedance: 20,000-Ω/V
Oscilloscope	Tektronix 454	Bandwidth: 130-MHz, sensitivity 50-mV/div, including probe
Low-Frequency oscillator	GR 1310	Min. Freq: 2 Hz, variable output attenuator
High-Frequency oscillator	GR 1211	Freq: 2 MHz–20 MHz, variable output attenuator
Standard Frequency oscillator	GR 1115-C	1 MHz, 1 V rms output

*Or equivalent

5.6.3 Power Supplies (Figure 5-1 and 6-4).

+5-V dc Power Supply. Use a dc voltmeter to measure the following voltages.

The +5-V dc regulator board is mounted vertically on the inside rear chassis. Take readings at the board terminals.

Measure +5-V dc to chassis ground at AT509: If adjustment is required, see calibration procedures.

If +5-V dc at AT509 is missing: Check for approximately 12-V dc between AT510 (–) and AT509 (+).

If 12-V dc at AT509–510 is missing: Use an ac voltmeter to measure approximately 11-V dc between AT505 and AT506.

If 11-V ac is missing: Check T501, S501, F501 and F502.

If 11-V ac is present: Check bridge-rectifier components CR501–CR504.

If 12-V dc is observed between AT509 and AT510: Check Q501–Q505 and associated components.

(+) and (–) 15-V dc Power Supply:

NOTE

The –15-V dc output must be present for the +15-V dc supply to operate.

Measure –15-V dc from pin 1 of SO502 to chassis ground.

If –15-V dc is missing at SO502-1: Measure approximately 45-V dc between the junctions of CR551/CR552 (–) and CR553/CR554 (+).

If 45-V dc is missing: Use an ac voltmeter to measure 40-V ac between pins 22 and 24 of SO502.

If 40-V ac is missing: Check T501, S501, F501 and F502.

If 40-V ac is present: Check bridge-rectifier components CR551–CR554.

If approximately 45-V dc is present at the bridge output: Check regulator transistors Q555–Q558 and associated components.

Measure +15-V dc to chassis ground at SO502-8.

If +15-V dc is missing: Check –15-V dc supply.

If –15-V dc is present: Check Q551–Q553 and associated components.

If –15-V dc is missing: Perform the preceding –15-V dc power supply troubleshooting steps.

NOTE

The –15-V dc supply contains a voltage output level adjustment. The +15-V dc supply has no adjustment and is referenced to the –15-V dc supply. See calibrating procedures for power supply adjustments.

Paragraph 4.4.1 contains the detailed operational theory for the power supplies.

5.6.4 Crystal Oven.

See Figures 5-1 and 6-5. The crystal oven contains the crystal, a thermistor and a heater. Take test readings at the pins of SO902. Refer to Table 5-3 for test voltage readings.

TABLE 5-3

VOLTAGE READINGS

Pin	Circuit	dc Voltage
1	THERMISTOR	+5V
2	+15V SUPPLY	+15V
3	CRYSTAL	0V
4	NC	–––
5	CRYSTAL (VARACTOR BIAS)	3.6V
6	NC	–––
7	HEATER	6V (Varies with Ambient Temp)
8	GND	0V

5.6.5 Input Circuits.

See Figure 6-6. Apply a signal from any stable, convenient source to INPUT jack (J901 or J902). Connect an oscilloscope with EXT SYNC, to the signal frequency and observe signal CN at pin 24. Signal CN should be the same frequency as the input signal.

NOTE

CN pulses are very narrow (15-ns) and may be difficult to observe at low signal frequencies.

Place SLOPE switch (S903) in both + and – position and observe CN pulses displaced in time by one half period.

If CN not observed: Check input signal frequency at the input jacks.

If signal observed at input jacks: Check Q113 collector for signal frequency.

If signal observed at Q113 collector: Check slope gate circuits, IC101A, IC101F, IC102A–IC102D and associated components.

If signal not observed at Q113 collector: Check Q110 collector for signal.

If signal observed at Q110 collector: Check Schmitt-trigger circuit (Q111–Q114 and Components).

If signal not observed at Q110 collector: Check for signal at Q106 collector.

If signal observed at Q106: Check Q115, Q104 and Q102.

If signal not observed at Q106: Check Q102 collector.

If signal observed at Q102: Check Q105, Q106.

If signal not observed at Q102: Check Q101 and input circuitry.

NOTES

1. If noise triggering becomes a problem resulting in instability check the bandswitch gating circuits (Q103/IC101B, Q104/IC101C, Q107/101D and Q108/IC101E).
2. Refer to paragraph 4.4.3 for detailed theory of operation.

5.6.6 Clock Circuits.

See Figure 6-5.

10-MHz Clock Check. Connect a signal frequency to the signal input jack (J901, J902). Select a signal frequency of 1-kHz or higher. Place the MEAS RATE switch (S904) to FAST. Use a dual-trace oscilloscope to observe the following signals.

Observe signal CT at pin 12 for blocks of 10-MHz pulses.

If no CT signal observed: Check TP601 for a 10-MHz sinusoidal signal. (TP601 is located on the lower left corner on the etched side of the board and is a protruding eyelet and terminal).

If no 10-MHz signal observed at TP601: Check oscillator (Q601—Q602), crystal oven and oven control circuits.

If 10-MHz signal observed at TP601: Check for 10-MHz pulses at IC607 pin 2.

If 10-MHz not observed at IC607-2: Check IC601A (shaper).

If 10-MHz observed at IC607-2: Check pin 13 for gate signal G. (G is a high level during the count cycle).

If signal G not observed: Troubleshoot Gate board.

If signal G is observed: Check gates IC604A and IC607C.

1-MHz Clock Check. Apply an input signal frequency of 5-Hz to input jack (J901 or J902). Place MEAS RATE switch (S904) to the SLOW position. Check pin 12 (signal CT) for 1-MHz pulses.

If 1-MHz pulses not observed: Check IC602, pin 11 for 1-MHz pulse signal.

If 1-MHz pulses observed at IC602-11: Check gates IC607B and IC604A.

If 1-MHz pulses not observed at IC602-11: Check IC602-14 for 10-MHz pulses.

If 10-MHz pulses observed at IC602-14: Replace IC602.

Clock Logic Check. Apply an input signal to J901/J902 INPUT from a low frequency test oscillator. Place MEAS RATE switch (S904) to AUTO. Set the oscillator frequency to 5-Hz.

Observe a high (ONE) dc level at IC606-14.

Raise the test oscillator frequency to above 8-Hz.

Observe a low (ZERO) level at IC606-14.

If the preceding indications not observed at IC606-14: Troubleshoot the clock logic circuits (IC606A, IC604B, IC605A, IC605B, IC608B). Refer to detailed operational theory in paragraph 4.4.4.

5.6.7 Gate Circuits.

See Figure 6-7. Apply a signal frequency to INPUT jack (J901/J902) of 1 kHz or greater. Use an oscilloscope to observe the following signals.

Check pin 2 for signal CNG (gated count) at the signal frequency.

If CNG is not observed: Check pin 5 for signal CN (continuous input signal frequency) and pin 7 for gate signal (G).

If CN and G are observed: Check gates IC158C/D.

If G is not observed: Check IC157 flip-flop and display control circuits.

See paragraph 4.4.5 for detailed functional theory of the Gate Circuit board.

5.6.8 Shift/Count Registers Circuits.

See Figure 6-8. Apply a signal of 1 MHz or greater to input jack J901/J902. Observe the following indications on an oscilloscope.

NOTE

To observe the compute- or count-cycle signals, synchronize the oscilloscope on signal RC. Successive divisions-by-two can then be observed at each flip-flop output.

Figure 5-3 presents a block diagram illustrating the operation of the Time (T) and Period (P) registers (see Section 4 for circuit details).

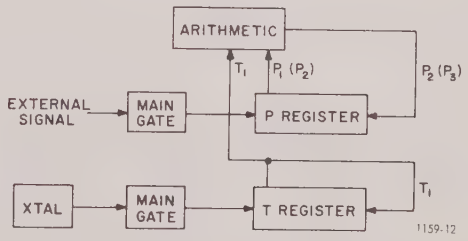


Figure 5-3. Shift/Count Registers Circuits block diagram.

The external signal is loaded into the P register (via the Main Gate) while the T register is loaded (also via a Main Gate) from the crystal. The contents of both registers (binary numbers P_1 and T_1) are shifted into the arithmetic circuits where T_1 is subtracted from P_1, producing P_2; P_2 and T_1 are then loaded into the registers. The sequence continues with the shifting of P_2 and T_1 into the arithmetic circuits, the subtraction of T_1 from P_2, and the production of P_3.

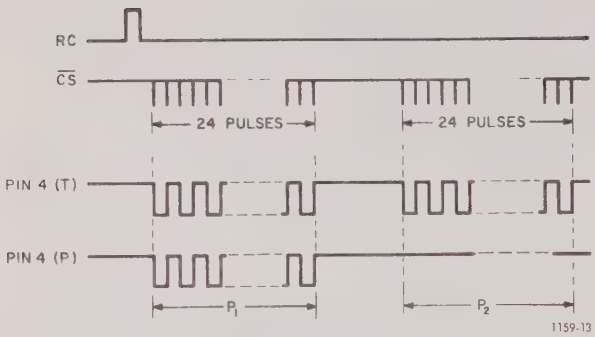


Figure 5-4. Test example.

Convenient inputs can be selected for test purposes; if $P_1 = T_1$, then $P_2 = P_1 - T_1 = 0$, and $P_3 = P_2 - T_1 = -T_1$. Figure 5-4 shows a sample where P_1 and T_1 consist of alternating 1's and 0's.

5.6.9 Arithmetic Program Circuits.

See Figure 6-9.

Input Signals Check. Apply an input signal of 1-kHz or greater to the INPUT jack (J901/J902). Use an oscilloscope to observe the following signals. Synchronize the oscilloscope on the RC signal.

Check pins 3 and 21 for signals NQ1 and $N\overline{Q1}$ from the period register. (The signals are binary ONES and ZEROES and are not symmetrical.)

Check pins 6 and 7 for signals TQ1 and $T\overline{Q1}$ from the time register. (The signals are binary ONES and ZEROES and are not symmetrical.)

Check pin 20 for the CP signal pulses.

Output Signals Check. Observe $\overline{CD}$ pulses at pin 4 to DCU enable flip-flops in Quotient Registers A and B.

Observe CF Pulses to Quotient Registers A and B DCU's at pin 22.

Observe DC and $\overline{DC}$ pulses at pins 15 and 14.

Observe SUM and $\overline{SUM}$ output pulses at pins 9 and 10.

Refer to paragraph 4.4.7 for detailed functional theory of the Arithmetic Program Circuits.

5.6.10 Quotient Register A Circuits.

See Figure 6-10. Apply an input signal of 1 kHz or greater to INPUT jack (J901/J902). Use an oscilloscope to observe the following signals. Synchronize oscilloscope on RC signal.

Check pins 9 through 20 for output pulses to display indicator decoder/drivers.

If no pulses observed at any one terminal: Check the associated output NAND gate.

If a complete pulse group is not observed: (A, B, C, D) Check pin 14 of IC251, IC252 and IC263 (DCU's) for CF pulses.

If CF pulses not observed at DCU: Check flip-flops (IC254 and IC256B and C) with associated gates.

Input Signals Check.

Observe $\overline{CD}$ pulses at pin 4.

Observe $\overline{ABT}$ as a high (ONE) level at pin 3.

Observe RC at pin 8.

See paragraph 4.4.8 for detailed operational theory of Quotient Register A.

5.6.11 Quotient Register B Circuits.

See Figure 6-10. Apply an input signal of 1 kHz or greater to INPUT jack (J901/J902). Use an oscilloscope to observe the following signals. Synchronize oscilloscope on RC signal.

Check pins 9 through 20 for output pulses to display indicator decoder drivers.

If no pulses observed at any one terminal: Check the associated output NAND gate.

If a complete pulse group is not observed: (A, B, C, D) Check pin 14 of IC302, IC304, IC306, and pin 1 of IC309 (DCU's) for CF pulses.

If CF Pulses not observed at DCU: Check flip-flops IC301 and IC308 with associated gates.

Input Signals Check.

Observe CD pulses at pin 7.

Observe RC and $\overline{RC}$ pulses at pins 6 and 8.

Observe CF pulses at pin 22.

Observe QA pulses at pin 23.

Observe $\overline{RA}$ pulses at pin 5.

Output Signals Check.

Observe QC at pin 3.

See paragraph 4.4.9 for detailed theory of operation for Quotient Register B circuits.

5.6.12 Add Cycle and Reset Circuits.

See Figure 6-11. Connect a signal frequency of 1 kHz or higher to the INPUT jack (J901/J902). Use an oscilloscope to observe the following signals. Synchronize oscilloscope with RC pulse to observe compute cycle signals.

Divide-by-32 Counter Check. Check pin 20 for CP pulses.

If no CP pulses at A945-20: Check pin 23 for 5-MHz CA clock pulses.

If signal CA is not observed: Troubleshoot Clock Circuit board.

If signal CA is observed: Check pins 15 and 17 for gate signals DC and QC.

If DC is not observed: Troubleshoot Arithmetic Program board.

If QC is not observed: Troubleshoot Quotient Register B board.

If DC and QC are observed: Check the outputs of the divide-by-32 counter flip-flops (IC456, IC458, IC460) and associated gates.

Reset A Circuit Check: Check pins 13 and 19 for signals RA and $\overline{RA}$ respectively.

If RA is observed; $\overline{RA}$ not observed: Gate IC457A is defective.

If RA is not observed: Check flip-flop IC454 and associated gates.

Reset C Circuit Check: Check pin 8 for signal RC.

RC not observed: Check pin 11 for signal $\overline{G}$.

If signal $\overline{G}$ not observed: Troubleshoot Gate board.

If signal G is observed: Check flip-flop IC452 and associated gates.

See paragraph 4.4.10 for detailed operational theory of the Add Cycle and Reset Circuits.

5.6.13 Range Counter Circuits.

See Figure 6-12. Connect a signal frequency of 1 kHz or higher to the INPUT jack (J901/J902). Use an oscilloscope to observe the following signals. Synchronize oscilloscope with RC pulse to observe compute cycle signals.

Decimal Point Circuit Check. Check pins 13, 14 and 15 for level at DP3, DP4 and DP5 respectively. Change the frequency range to move the decimal point. One DP will be low (lighted), while the other two are high.

If one DP signal is missing: Check the output lamp driver (Q351, Q352, Q353) and associated NAND gate.

If DP3, DP4 and DP5 all missing: Check pin 7 for signal CD.

If CD is missing: Troubleshoot Arithmetic Program board.

If CD is observed: Check flip-flops (IC356) and associated gates.

Frequency Unit Circuit Check. Check pins 10, 12 and 16 for signals MHzI, kHzI and HzI respectively.

If one signal missing: Check output lamp driver (Q354, Q355, Q356) and associated gate.

If all signals missing: Check pin 7 for signal CD.

If CD is missing: Troubleshoot Arithmetic Program board.

If CD is present: Check flip-flops (IC357) and associated gates.

NOTE

Remove the signal source from INPUT jack.

Observe signal NSI (+5-V dc) at pin 21.

If NSI is missing: Check pin 24 for signal $\overline{STG}$.

If $\overline{STG}$ is missing: Troubleshoot Gate board.

If STG is present: Check gates IC359—360, Q358 lamp driver and Q359.

Low Frequency Circuit Check.

NOTE

Place MEAS RATE switch in the FAST position with a signal input to J901/J902 of 5 Hz.

Check pin 18 for signal LFI (+5-V dc level).

If LFI is missing: Check pin 14 for signal $\overline{RC}$; check pin 20 for signal $\overline{TOF}$; check pin 11 for signal $\overline{G}$.

If all signals present: Check gates 355, 358 and 360.

See paragraph 4.4.11 for detailed operational theory of the Range Counter Circuits.

5.6.14 Buffer Circuits.

See Figure 6-13. The Buffer Circuit board is an interface between SO930, SO925, SO935, SO945, SO960 and the data output connector, SO904.

Troubleshooting consists of checking inputs and outputs with reference to appropriate schematics.

5.6.15 Readout Circuits.

See Figure 6-10. Connect a signal source of 1 kHz or higher to the INPUT jack (J901/J902). Observe the following indications on an oscilloscope.

No readout is observed on indicators: Check SO701 pin 4 to ground with a dc voltmeter for approximately +240-V dc.

If +240-V dc missing: Check T501 and rectifier components on readout board.

If +240-V dc is present: Check Q701 collector for ZERO level gates.

If no ZERO level gates observed: Check AT735 for signal $\overline{GC}$.

If $\overline{GC}$ is missing: Troubleshoot Gate board.

If $\overline{GC}$ is present: Check Q701 and associated components.

NOTE

A defective decoder/driver (IC701 through IC706) may give erroneous indications.

If a correct BCD input is present the decoder/driver may be defective and must be checked.

See paragraph 4.4.13 for detailed operational theory of the Readout Circuit board.

5.7 CALIBRATION.

5.7.1 General.

The 1159 does not require routine periodic calibration. The modules that require calibration are the:

1. +5-V dc power supply
2. −15-V dc power supply
3. 10-MHz crystal oscillator on Clock board.

Refer to Figures 5-1 and 5-2 for the location of calibrating adjustments.

Refer to Table 5-2 for test equipment.

5.7.2 +5-V dc Power Supply.

The voltage level adjustment is R502.

a. Connect a dc voltmeter between terminals 509 (+) and 512 (−) to read +5-V dc.

b. Adjust R502 for a voltmeter reading of exactly +5-V dc.

5.7.3 −15-V dc Power Supply.

The voltage level adjustment for the −15-V dc power supply is R569.

a. Connect a dc voltmeter from SO502-1 to chassis ground to read −15-V dc.

b. Adjust R569 for a voltmeter reading of exactly −15-V dc.

5.7.4 +15-V dc Power Supply.

Connect a dc voltmeter from SO502-8 to chassis ground to read +15-V dc.

a. If the +15-V dc reading is in error after calibrating the −15-V dc supply, troubleshoot all components of the +15-V dc supply.

5.7.5 10-MHz Clock Oscillator.

Accurate tests should be made in comparison with a frequency standard that exceeds the listed specifications of the 10-MHz oscillator, before attempting calibration. Ensure that a suitable warm-up time period has elapsed before performing calibrating procedures.

The oscillator 10-MHz output is measured at TP601 on the Clock Circuit board with no external standard frequency (phase-lock) applied to J903.

Tune C901 for frequency and L601 for output amplitude.

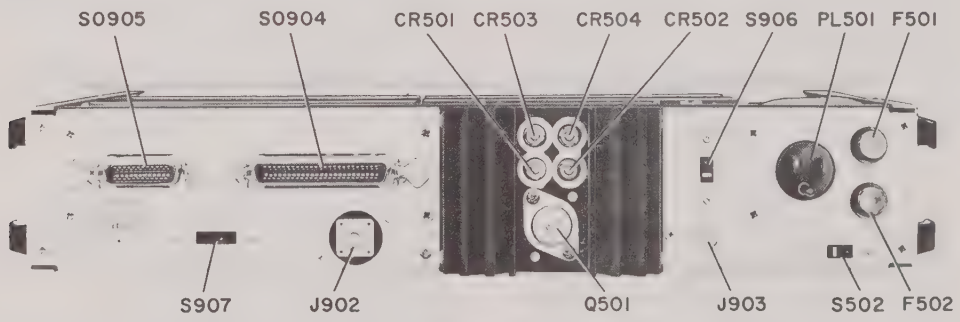


Figure 5-5. Rear panel part identification.

Parts Lists and Diagrams—Section 6

INDEX OF DIAGRAMS

FEDERAL MANUFACTURER'S CODES
SIGNAL INDEX

Figure 6-1 Block Diagram

Figure 6-2 Timing and Detailed Logic Diagrams

Figure 6-3 Interconnections

Figure 6-4 Power Supplies-Schematics, Etched Boards, and Parts Lists

Figure 6-5. Crystal Oven, Oven Control, and Clock—Schematics, Etched Boards, and Parts Lists.

Figure 6-6 Input-Schematics, Etched Boards, and Parts Lists

Figure 6-7 Gate-Schematic, Etched Boards, and Parts Lists

Figure 6-8 Shift/Count Register-Schematic, Etched Boards, and Parts Lists

Figure 6-9 Arithmetic Program-Schematic, Etched Boards, and Parts Lists

Figure 6-10 Quotient Registers and Readout-Schematic, Etched Boards, and Parts Lists

Figure 6-11 Add Cycle and Reset-Schematic, Etched Boards, and Parts Lists

Figure 6-12 Range Counter-Schematic, Etched Boards, and Parts Lists

Figure 6-13 Buffer-Schematic, Etched Boards and Parts Lists

Figure 6-14 Controls Wiring

SIGNAL INDEX

SIGNAL	FUNCTION
ABT	ABORT; generates reset when clock speed changes
CA	5-MHz clock signal
CD	Clock pulse D; generated by end of arithmetic cycle and pulse CP.
CF	Clock pulse F; generated by subtract, carry and pulse CP. Drives quotient registers DCU's.
CN	Count signal; pulse output of input circuit.
CNG	Gated count signal to period register.
CP	Cycle pulse; cycles arithmetic program counter.
CS	5-MHz shift pulses; shift information from time and period registers.
CT	Time register clock; either 1-MHz or 10-MHz.
DC	Cycle counter disable.
DP3	Decimal point 3.
DP4	Decimal point 4.
DP5	Decimal point 5.
DTA	Display time A — starts display.
DTB	Display time B — ends display.
EXT	External reference standard of 100-kHz or 1 MHz.
G	Count enable gate.
$\bar{G}$	Compute enable gate.
GCS	Shift pulse gate.
GND	Chassis ground.
Hzl or Z	Hz lamp drive signal.
kHzl or Y	kHz lamp drive signal.
LFI	LOW FREQUENCY lamp-drive signal.
$\overline{LG}$	Low-speed clock (1-MHz) gate from MEAS RATE switch (S904).
MHzl	Drive signal to MHz indicator lamp.
NSI	NO SIGNAL lamp drive.
NQ1–NQ24	Q outputs of period register.
$N\bar{Q}1$–$N\bar{Q}24$	$\bar{Q}$ outputs of period register.
$\overline{PC}$	Print command to data output connector.
PIN	Printer inhibit to Type 1137 printer.
PCT	Print command termination. Supplied by some output devices for synchronous operation.

SIGNAL	FUNCTION
QA	Quotient A decade enable to Quotient B.
QC	End of quotient decade cycle.
RA	Reset A; end of compute cycle.
RC	Reset C; end of count cycle.
$\overline{RM}$	Manual reset.
RTLA	Remote controlled trigger level amplitude from R901/S908.
$\overline{SG}$	Fast speed clock (10-MHz) gate from MEAS RATE switch (S904).
SLP	Slope select signal from S903.
STG	Start gate for count cycle.
TLA	Trigger level amplitude from R901/S908.
TG1	100-kHz reference standard gate from S906.
TG2	1-MHz reference standard gate from S906.
$\overline{TOF}$	Time counter-overflow; generates abort.
TQ1–TQ24	Q outputs of time register.
$T\bar{Q}1$–$T\bar{Q}24$	$\bar{Q}$ outputs of time register.
XTAL1–XTAL2	Crystal inputs to 10-MHz clock oscillator.
Y	Same as kHzl.
Z	Same as Hzl.
1KF	1-kHz filter gate enable from bandswitch.
10KF	10-kHz filter gate enable from bandswitch.
100KF	100-kHz filter gate enable from bandswitch.
1MF	1-MHz filter gate enable from bandswitch.
10X	Prescaler factor (10:1).
100X	Prescaler factor (100:1).
10MG	10-MHz clock gate.
1F$\bar{A}$–1F$\bar{D}$	BCD outputs to indicator 1.
2F$\bar{A}$–2F$\bar{D}$	BCD outputs to indicator 2.
3F$\bar{A}$–3F$\bar{D}$	BCD outputs to indicator 3.
4F$\bar{A}$–4F$\bar{D}$	BCD outputs to indicator 4.
5F$\bar{A}$–5F$\bar{D}$	BCD outputs to indicator 5.
6F$\bar{A}$–6F$\bar{D}$	BCD outputs to indicator 6.

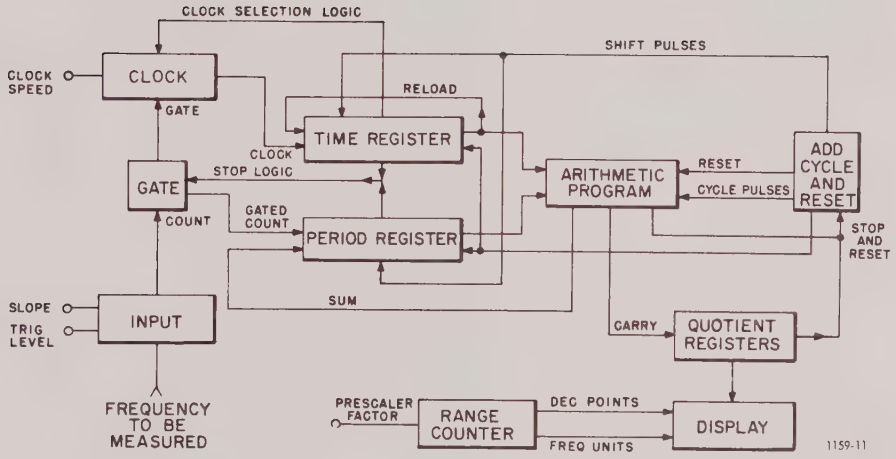


Figure 6-1. Block Diagram.

Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
Braided Cable Assembly	1159-0200	24655	1159-0200	
Braided Cable Assembly	1159-0210	24655	1159-0210	
Braided Cable Assembly	1159-0220	24655	1159-0220	
Braided Cable Assembly	1159-0230	24655	1159-0230	
Braided Cable Assembly	1159-0240	24655	1159-0240	
Braided Cable Assembly	1159-0250	24655	1159-0250	
Lead Set	1159-0260	24655	1159-0260	
Guide Bracket Assembly	1159-1070	24655	1159-1070	
Guide Bracket Assembly	1159-1080	24655	1159-1080	
Guide Bracket Assembly	1159-1090	24655	1159-1090	
Dress Panel Assembly Marked	1159-1801	24655	1159-1801	
Window Marked	1159-7011	24655	1159-7011	
Window	1159-7010	24655	1159-7010	
Control Panel Marked	1159-8131	24655	1159-8131	
Lamp Bracket	1159-8160	24655	1159-8160	
Heat Sink	1159-8250	24655	1159-8250	
Stop-Part of Pan Assemblies	4171-7040	24655	4171-7040	
Slide Block	4171-7050	24655	4171-7050	
Cabinet Assembly- Bench Model	4173-4000	24655	4173-4000	
Hardware Set- Rack	4174-2000	24655	4174-2000	
Cabinet Assembly-Rack	4174-3990	24655	4174-3990	
Power Cord	4200-9622	24655	4200-9622	
Connector, Etched Circuit	4215-2034	24655	4215-2034	
Handle, rack instrument	5360-2007	24655	5360-2007	
Knob Assembly- Time Level	5500-5131	24655	5500-5131	
Knob Assembly-Input Band	5500-5131	24655	5500-5131	
Knob Assembly-Display Time	5500-5131	24655	5500-5131	
Lamp Holder	5600-1021	24655	5600-1021	
Mounting Device Fuse	5650-0100	24655	5650-0100	
Switch Cap	7915-1000	24655	7915-1000	
Switch Cap Spring	7915-2000	24655	7915-2000	
Oven Assembly	1158-4000	24655	1158-4000	
Readout Circuit Assembly	1159-2771	24655	1159-2771	
5 V Reg. Circuit Assembly	1159-2781	24655	1159-2781	
Input Circuit Assembly	1159-4711	24655	1159-4711	
Gate Circuit Assembly	1159-4715	24655	1159-4715	
Shift-Count Reg. Circuit	1159-4720	24655	1159-4720	
Quotient Reg. A Circuit	1159-4725	24655	1159-4725	
Quotient Reg. B Circuit	1159-4730	24655	1159-4730	
Range Counter Circuit	1159-4735	24655	1159-4735	
Arith. Program Circuit	1159-4740	24655	1159-4740	
Add Cycle + Reset Circuit	1159-4745	24655	1159-4745	
Recipromatic Counter	1159-4756	24655	1159-4756	
Clock Circuit Asm.	1159-4760	24655	1159-4760	
Oven Control Circuit	1159-4765	24655	1159-4765	

CHASSIS MOUNTED COMPONENTS

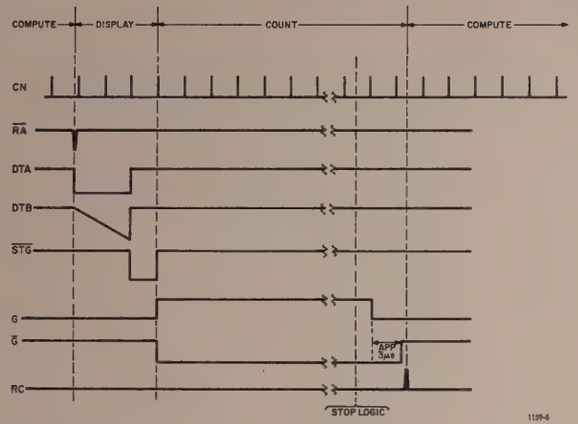
Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
C901	Trimmer, 10-100 pF, 500 V	4910-0700	71590	823-BN 10-100 pF	
C902	Mica, 15 pF ±5% 500 V	4040-0100	72136	CM15, 15 pF ±5%	
C903	Tantalum, 10 µF ±20% 20 V	4450-5100	56289	150D106X0020B2	5910-855-6343
C904	Tantalum, 47 µF ±20% 6 V	4450-5500	56289	150D476X0006B2	5910-752-4185
C905	Tantalum, 10 µF ±20% 20 V	4450-5100	56289	150D106X0020B2	5910-855-6343
C906	Tantalum, 47 µF ±20% 6 V	4450-5500	56289	150D476X0006B2	5910-752-4185
C907	Tantalum, 47 µF ±20% 6 V	4450-5500	56289	150D476X0006B2	5910-752-4185
CR901	Type 1N995	6082-1002	80368	1N995	
L901	Inductor, 2.2 µH ±10%	4300-1200	99800	1537-20, 2.2 µH ±10%	
L902	Inductor, 22 µH ±10%	4300-6600	99800	2890, 22 µH ±10%	
L903	Inductor, 22 µH ±10%	4300-6600	99800	2890, 22 µH ±10%	
R901	Potentiometer, Composition, 100 kΩ ±10%	6045-2041	01121	JJ, 100 kΩ ±10%	
R902	Potentiometer, Composition, 100 kΩ ±10%	6045-2040	01121	JJ, 100 kΩ ±10%	
R903	Composition, 100 kΩ ±10%	6099-4109	75042	BTS, 100 kΩ ±10%	
R904	Composition, 20 kΩ ±5%	6099-3205	75042	BTS, 20 kΩ ±5%	5905-686-3368
R905	Composition, 56 kΩ ±10%	6099-3569	75042	BTS, 56 kΩ ±10%	
S901	Pushbutton	7870-1511	81073	4001 N. O.	
S902	(Part of R902)				
S903	Toggle	7910-0790	95146	MST-105D	
S904	Toggle	7910-0810	95146	MST-105E	
S905	Rotary Wafer	7890-5110	24655	7890-5110	
S906	Slide	7910-0831	42190	4603	
S907	Slide	7910-1660	82389	13037	
S908	(Part of R901)				
P901 thru P905	Lamp	5600-0300	24454	#328	6240-155-7857
J901	874 Type	0874-4622	24655	0874-4622	
J902	BNC Type	4230-2320	24655	4230-2320	
J903	BNC Type, Single Hole	4230-2300	81349	UG-1094/U	
SO901	EC, 6 position	4230-2706	95354	CD606SF	
SO902	EC, 34 positions	7530-2700	81350	TS101P02	5935-129-9358
SO903	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO904	Multiple Socket, 50 connectors	4230-4050 or 4049	24655	4230-4050	
SO905	Multiple Socket, 24 connectors	4230-4024	93916	57-40240	
SO910	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO915	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO921 thru SO925	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO930	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO935	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO940	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO945	EC, 24 positions	4230-2724	95354	91-6024-1201-00	
SO960	EC, 24 positions	4230-2724	95354	91-6024-1201-00	

FEDERAL MANUFACTURER'S CODE

From Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) as supplemented through August, 1968.

Code	Manufacturer
00192	Jones Mfg. Co, Chicago, Illinois
00194	Waisco Electronics Corp, L.A., Calif.
00434	Schweber Electronics, Westburg, L.I., N.Y.
00656	Aerovox Corp, New Bedford, Mass.
01009	Alden Products Co, Brockton, Mass.
01121	Allen-Bradley, Co, Milwaukee, Wisc.
01295	Texas Instruments, Inc, Dallas, Texas
02114	Ferroxcube Corp, Saugertles, N.Y. 12477
02606	Fenwal Lab Inc, Morton Grove, Ill.
02660	Amphenol Electron Corp, Broadview, Ill.
02768	Fastex, Des Plaines, Ill. 60016
03508	G.E. Semicon Prod, Syracuse, N.Y. 13201
03636	Grayburne, Yonkers, N.Y. 10701
03888	Pyrofilm Resistor Co, Cedar Knolls, N.J.
03911	Clairex Corp, New York, N.Y. 10001
04009	Arrow-Hart & Hegeman, Hartford, Conn. 06106
04713	Motorola, Phoenix, Ariz. 85008
05170	Engr'd Electronics, Santa Ana, Calif. 92702
05624	Barber-Colman Co, Rockford, Ill. 61101
05820	Wakefield Eng, Inc, Wakefield, Mass. 01880
07126	Digitron Co, Pasadena, Calif.
07127	Eagle Signal (E.W. Bliss Co), Baraboo, Wisc.
07261	Avnet Corp, Culver City, Calif. 90230
07263	Fairchild Camera, Mountain View, Calif.
07387	Birtcher Corp, No. Los Angeles, Calif.
07595	Amer Semicond, Arlington Hts, Ill. 60004
07828	Bodine Corp, Bridgeport, Conn. 06605
07829	Bodine Electric Co, Chicago, Ill. 60618
07910	Cont Device Corp, Hawthorne, Calif.
07983	State Labs Inc, N.Y., N.Y. 10003
07999	Borg Inst., Delavan, Wisc. 53115
08730	Vemaline Prod Co, Franklin Lakes, N.J.
09213	G.E. Semiconductor, Buffalo, N.Y.
09408	Star-Tronics Inc, Georgetown, Mass. 01830
09823	Burgess Battery Co, Freeport, Ill.
09922	Burndy Corp, Norwalk, Conn. 06852
11236	C.T.S. of Berne, Inc, Berne, Ind. 46711
11599	Chandler Evans Corp, W. Hartford, Conn.
12040	National Semiconductor, Danbury, Conn.
12498	Crystalonics, Cambridge, Mass. 02140
12672	RCA, Woodbridge, N.J.
12697	Clarostat Mfg Co, Inc, Dover, N.H. 03820
12954	Dickson Electronics, Scottsdale, Ariz.
13327	Solitron Devices, Tappan, N.Y. 10983
14433	ITT Semicondictors, W.Palm Beach, Fla.
14655	Cornell-Dubilier Electric Co, Newark, N.J.
14674	Corning Glass Works, Corning, N.Y.
14936	General Instrument Corp, Hicksville, N.Y.
15238	ITT, Semiconductor Div, Lawrence, Mass.
15605	Cutlet-Hammer Inc, Milwaukee, Wisc. 53233
16037	Spruce Pine Mica Co, Spruce Pine, N.C.
17771	Singer Co, Diehl Div, Somerville, N.J.
19396	Illinois Tool Works, Pakton Div, Chicago, Ill.
19644	LRC Electronics, Horseheads, N.Y.
19701	Electra Mfg Co, Independence, Kansas 67301
21335	Fafnir Bearing Co, New Briton, Conn.
22753	UID Electronics Corp, Hollywood, Fla.
23342	Avnet Electronics Corp, Franklin Park, Ill.
24446	G.E., Schenectady, N.Y. 12305
24454	G.E., Electronics Comp, Syracuse, N.Y.
24455	G.E. (Lamp Div), Nela Park, Cleveland, Ohio
24655	General Radio Co, W. Concord, Mass. 01781
26806	American Zettlet Inc, Costa Mesa, Calif.
28520	Hayman Mfg Co, Kenilworth, N.J.
28959	Hoffman Electronics Corp, El Monte, Calif.
30874	I.B.M, Armonk, New York
32001	Jensen Mfg. Co, Chicago, Ill. 60638
33173	G.E. Comp, Owensboro, Ky. 42301
35929	Constanta Co, Mont. 19, Que.
37942	P.R. Mallory & Co Inc, Indianapolis, Ind.
38443	Marlin-Rockwell Corp, Jamestown, N.Y.
40931	Honeywell Inc, Minneapolis, Minn. 55408
42190	Muter Co, Chicago, Ill. 60638
42498	National Co, Inc, Melrose, Mass. 02176
43991	Norma-Hoffman, Stanford, Conn. 06904
49671	RCA, New York, N.Y. 10020
49956	Raytheon Mfg Co, Waltham, Mass. 02154
53021	Sangamo Electric Co, Springfield, Ill. 62705
54294	Shallcross Mfg Co, Selma, N.C.
54715	Shure Brothers, Inc, Evanston, Ill.
56289	Sprague Electric Co, N. Adams, Mass.
59730	Thomas and Betts Co, Elizabeth, N.J. 07207
59875	TRW Inc, (Accessories Div), Cleveland, Ohio
60399	Torrington Mfg Co, Torrington, Conn.
61637	Union Carbide Corp, New York, N.Y. 10017
61864	United-Carr Fastener Corp, Boston, Mass.
63060	Victoreen Instrument Co, Inc, Cleveland, O.
63743	Ward Leonard Electric Co, Mt. Vernon, N.Y.
65083	Westinghouse (Lamp Div), Bloomfield, N.J.
65092	Weston Instruments, Newark, N.J.
70485	Atlantic-India Rubber, Chicago, Ill. 60607
70563	Amperite Co, Union City, N.J. 07087
70903	Belden Mfg Co, Chicago, Ill. 60644
71126	Bronson, Homer D, Co, Beacon Falls, Conn.
71294	Canfield, H.O. Co, Clifton Forge, Va. 24422
71400	Bussman (McGraw Edison), St. Louis, Mo.
71468	ITT Cannon Elec, L.A., Calif. 90031
71590	Centralab, Inc, Milwaukee, Wisc. 53212
71666	Continental Carbon Co, Inc, New York, N.Y.
71707	Coto Coil Co Inc, Providence, R.I.
71744	Chicago Miniature Lamp Works, Chicago, Ill.
71785	Cinch Mfg Co, Chicago, Ill. 60624
71823	Darnell Corp, Ltd, Downey, Calif. 90241
72136	Electro Motive Mfg Co, Wilmington, Conn.
72259	Nytronics Inc, Berkeley Heights, N.J. 07922
72619	Dialight Co, Brooklyn, N.Y. 11237
72699	General Instr Corp, Newark, N.J. 07104
72765	Drake Mfg Co, Chicago, Ill. 60656
72825	Hugh H. Eby Inc, Philadelphia, Penn. 19144
72962	Elastic Stop Nut Corp, Union, N.J. 07083
72982	Erie Technological Products Inc, Erie, Penn.
73138	Beckman Inc, Fullerton, Calif. 92634
73445	Amperex Electronics Co, Hicksville, N.Y.
73559	Carling Electric Co, W.Hartford, Conn.
73690	Elco Resistor Co, New York, N.Y.
73899	JFD Electronics Corp, Brooklyn, N.Y.
74193	Heinemann Electric Co, Trenton, N.J.
74861	Industrial Condenser Corp, Chicago, Ill.
74970	E.F. Johnson Co, Waseca, Minn. 56093
75042	IRC Inc, Philadelphia, Penn. 19108
75382	Kulka Electric Corp, Mt. Vernon, N.Y.
75491	Lafayette Industrial Electronics, Jamica, N.Y.
75608	Linden and Co, Providence, R.I.
75915	Littelfuse, Inc, Des Plaines, Ill. 60016
76005	Lord Mfg Co, Erie, Penn. 16512
76149	Mallory Electric Corp, Detroit, Mich. 48204
76487	James Millen Mfg Co, Malden, Mass. 02148
76545	Mueller Electric Co, Cleveland, Ohio 44114
76684	National Tube Co, Pittsburg, Penn.
76854	Oak Mfg Co, Crystal Lake, Ill.
77147	Patton MacGuyer Co, Providence, R.I.
77166	Pass-Seymour, Syracuse, N.Y.
77263	Pierce Roberts Rubber Co, Trenton, N.J.
77339	Positive Lockwasher Co, Newark, N.J.
77542	Ray-O-Vac Co, Madison, Wisc.
77630	TRW, Electronic Comp, Camden, N.J. 08103
77638	General Instruments Corp, Brooklyn, N.Y.
78189	Shakeproof (Ill. Tool Works), Elgin, Ill. 60120
78277	Sigma Instruments Inc, S.Braintree, Mass.
78488	Stackpole Carbon Co, St. Marys, Penn.
78553	Tinnerman Products, Inc, Cleveland, Ohio
79089	RCA, Rec Tube & Semicond, Harrison, N.J.
79725	Wiremold Co, Hartford, Conn. 06110
79963	Zierick Mfg Co, New Rochelle, N.Y.
80030	Prestole Fastener, Toledo, Ohio
80048	Vickers Inc, St. Louis, Mo.
80131	Electronic Industries Assoc, Washington, D.C.
80183	Sprague Products Co, No. Adams, Mass.
80211	Motorola Inc, Franklin Park, Ill. 60131
80258	Standard Oil Co, Lafeyette, Ind.
80294	Bourns Inc, Riverside, Calif. 92506
80431	Air Filter Corp, Milwaukee, Wisc. 53218
80583	Hammarlund Co, Inc, New York, N.Y.
80740	Beckman Instruments, Inc, Fullerton, Calif.
81030	International Insturment, Orange, Conn.
81073	Grayhill Inc, LaGrange, Ill. 60525
81143	Isolantite Mfg Corp, Stirling, N.J. 07980
81349	Military Specifications
81350	Joint Army-Navy Specifications
81751	Columbus Electronics Corp, Yonkers, N.Y.
81831	Filtron Co, Flushing, L.I., N.Y. 11354
81840	Ledex Inc, Dayton, Ohio 45402
81860	Barry-Wright Corp, Watertown, Mass.
82219	Sylvania Elec Prod, Emporium, Penn.
82273	Indiana Pattern & Model Works, LaPort, Ind.
82389	Switchcraft Inc, Chicago, Ill. 60630
82647	Metals & Controls Inc, Attleboro, Mass.
82807	Milwaukee Resistor Co, Milwaukee, Wisc.
83033	Meissner Mfg, (Maguire Ind) Mt. Carmel, Ill.
83058	Carr Fastener Co, Cambridge, Mass.
83186	Victory Engineering, Springfield, N.J. 07081
83361	Bearing Specialty Co, San Francisco, Calif.
83587	Solar Electric Corp, Warren, Penn.
83740	Union Carbide Corp, New York, N.Y. 10017
83781	National Electronics Inc, Geneva, Ill.
84411	TRW Capacitor Div, Ogallala, Nebr.
84835	Lehigh Metal Prods, Cambridge, Mass. 02140
84971	TA Mfg Corp, Los Angeles, Calif.
86577	Precision Metal Prods, Stoneham, Mass. 02180
86684	RCA (Elect. Comp & Dev), Harrison, N.J.
86687	REC Corp, New Rochelle, N.Y. 10801
86800	Cont Electronics Corp, Brooklyn, N.Y. 11222
88140	Cutler-Hammer Inc, Lincoln, Ill.
88219	Gould Nat. Batteries Inc, Trenton, N.J.
88419	Cornell-Dubilier, Fuquay-Varina, N.C.
88627	K & G Mfg Co, New York, N.Y.
89482	Holtzer-Cabot Corp, Boston, Mass.
89665	United Transformer Co, Chicago, Ill.
90201	Mallory Capacitor Co, Indianapolis, Ind.
90750	Westinghouse Electric Corp, Boston, Mass.
90952	Hardware Products Co, Reading, Penn. 19602
91032	Continental Wire Corp, York, Penn. 17405
91146	ITT (Cannon Electric Inc), Salem, Mass.
91293	Johanson Mfg Co, Boonton, N.J. 07005
91506	Augat Inc, Attleboro, Mass. 02703
91598	Chandler Co, Wethersfield, Conn. 06109
91637	Dale Electronics Inc, Columbus, Nebr.
91662	Elco Corp, Willow Grove, Penn.
91719	General Instruments, Inc, Dallas, Texas
91929	Honeywell Inc, Freeport, Ill.
92519	Electra Insul Corp, Woodside, L.I., N.Y.
92678	E.G.&G., Boston, Mass.
93332	Sylvania Elect Prods, Inc, Woburn, Mass.
93916	Cramer Products Co, New York, N.Y. 10013
94144	Raytheon Co, Components Div, Quincy, Mass.
94154	Tung Sol Electric Inc, Newark, N.J.
95076	Garde Mfg Co, Cumberland, R.I.
95121	Quality Components Inc, St. Mary's, Penn.
95146	Alco Electronics Mfg Co, Lawrence, Mass.
95238	Continental Connector Corp, Woodside, N.Y.
95275	Vitramon, Inc, Bridgeport, Conn.
95354	Methode Mfg Co, Chicago, Ill.
95412	General Electric Co, Schenectady, N.Y.
95794	Anaconda Amer Brass Co, Torrington, Conn.
96095	Hi-Q Div. of Aerovox Corp, Orlean, N.Y.
96214	Texas Instruments Inc, Dallas, Texas 75209
96256	Thordarson-Meissner, Mt. Carmel, Ill.
96341	Microwave Associates Inc, Burlington, Mass.
96791	Amphenol Corp, Jonesville, Wisc. 53545
96906	Military Standards
98291	Sealectro Corp, Mamaroneck, N.Y. 10544
98474	Compar Inc, Burlingame, Calif.
98821	North Hills Electronics Inc, Glen Cove, N.Y.
99180	Transitron Electronics Corp, Melrose, Mass.
99313	Varian, Palo Alto, Calif. 94303
99378	Atlee Corp, Winchester, Mass. 01890
99800	Delevan Electronics Corp, E. Aurora, N.Y.

9/68



Timing Diagram.

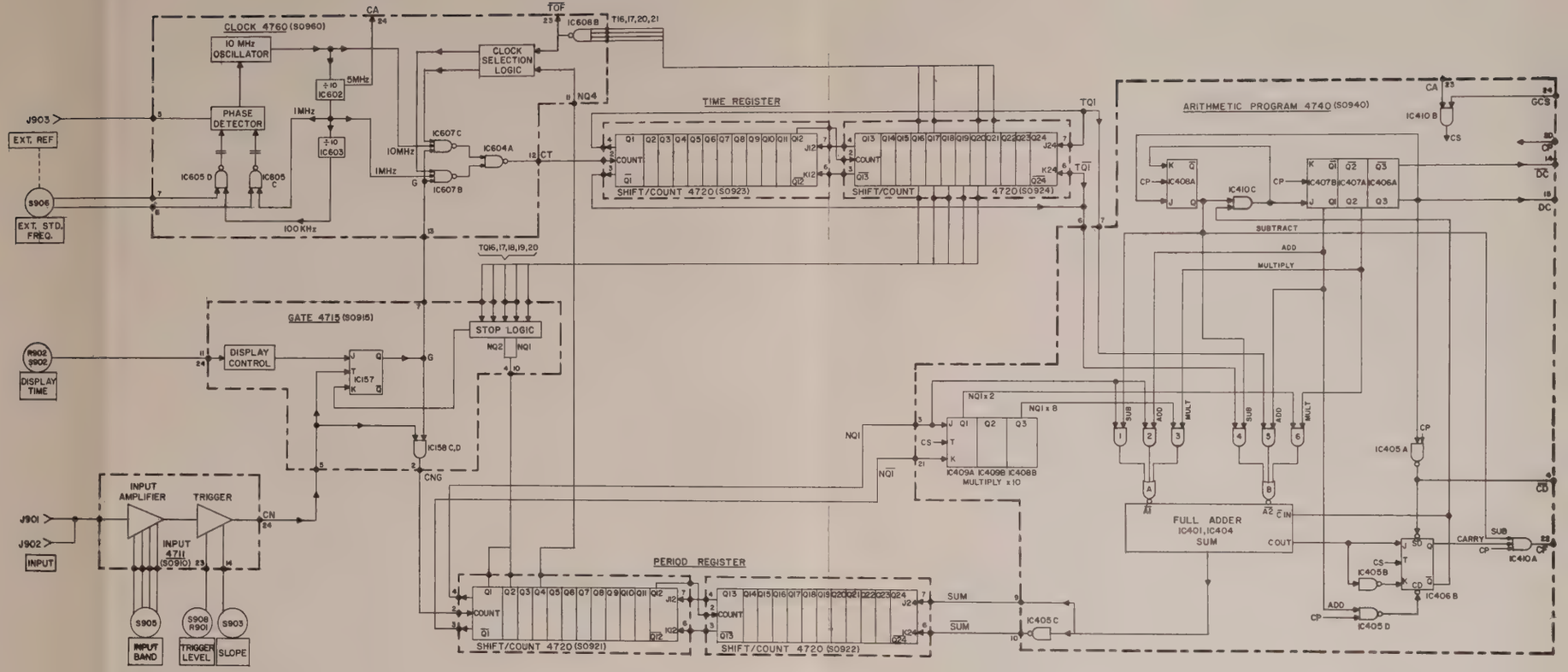


Figure 6-2A. 1159 Reciprocmatic Counter Logic Diagram (Part 1).

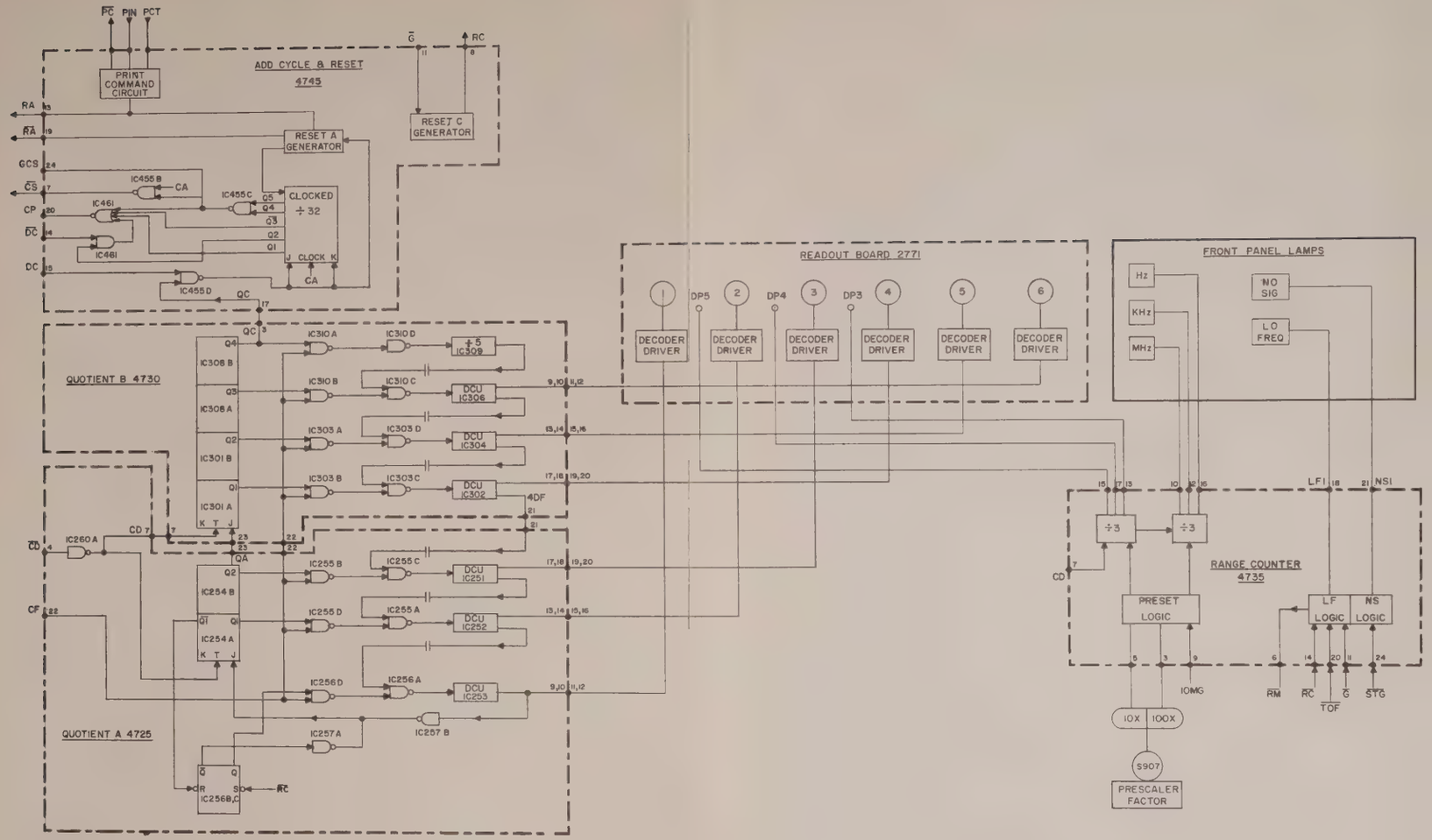
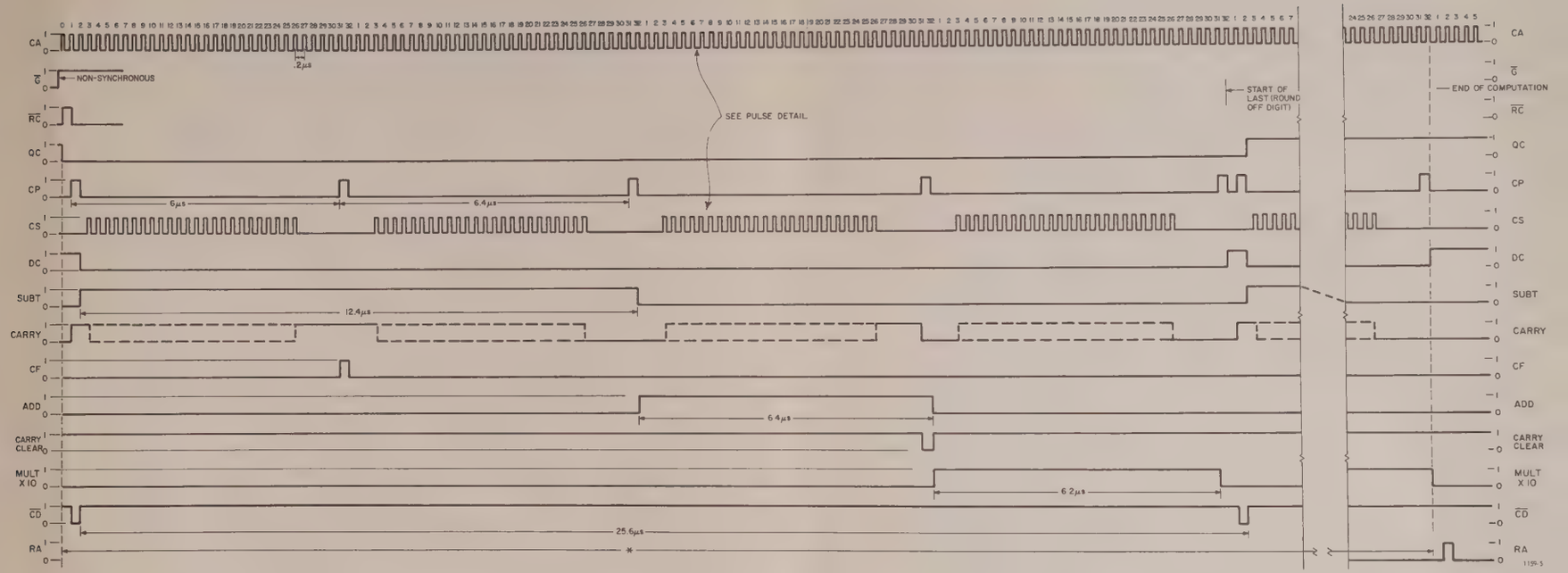
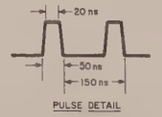


Figure 6-28. 1159 Reciprocmatic Counter Logic Diagram (Part 2).



* COMPUTATION LENGTH:
MINIMUM FOR 10.0000(0) MHz
22 CYCLES × 6.4 μs = 140.8 μs
MAXIMUM FOR 9.99999(9) Hz
105 CYCLES × 6.4 μs = 672 μs



PULSE DETAIL

Figure 6-2C. Timing Diagram.

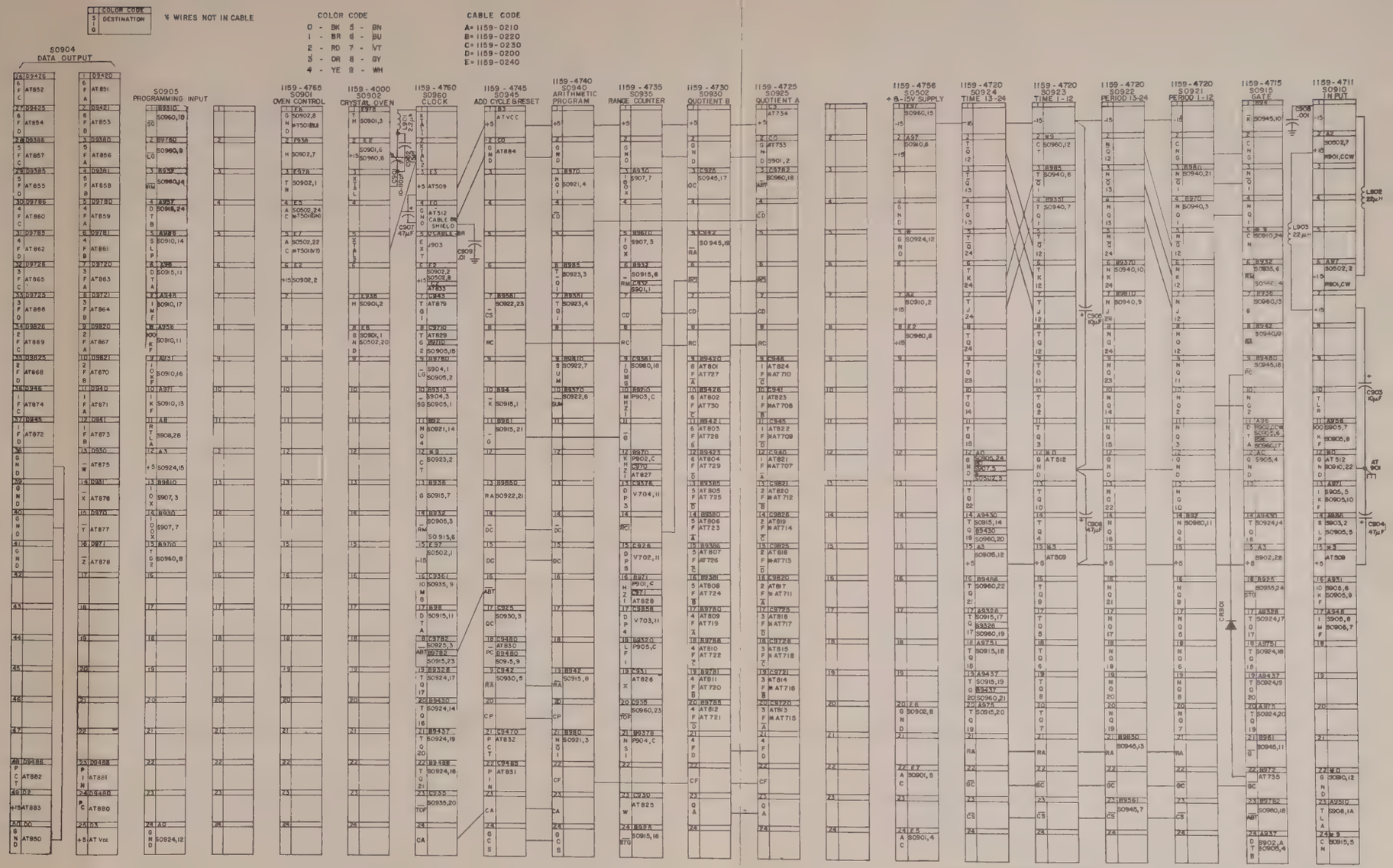


Figure 6-3. Interconnection Diagram.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C501	Electrolytic, 21,000 µF +75-10% 15 V	4450-6210	37942	TT, 21,000 µF +75-10%	
C502	Ceramic, 0.05 µF +80-20% 50 V	4403-3500	01121	40-503W	5910-883-7321
C503	Ceramic, 0.22 µF +80-20% 10 V	4432-4229	56289	29C365, .22 µF +80-20%	
C504	Tantalum, 47 µF ±20% 6 V	4450-5500	56289	150D476X0006B2	5910-752-4185
C551	Electrolytic, 660 µF +150-10% 25 V	4450-6125	37942	TT, 660 µF +150-10%	
C552	Electrolytic, 660 µF +150-10% 25 V	4450-6125	37942	TT, 660 µF +150-10%	
C553	Ceramic, 0.01 µF +80-20% 500 V	4406-3109	72982	811, 0.01 µF +80-20%	5910-977-7579
C554	Electrolytic, 60 µF +150-10% 25 V	4450-2900	56289	D17872	5910-799-9280
C555	Ceramic, 0.01 µF +80-20% 500 V	4406-3109	72982	811, 0.01 µF +80-20%	5910-977-7579
C556	Electrolytic, 33 µF ±20% 10 V	4450-5400	56289	150D336X0010B1	5910-823-1623
C557	Electrolytic, 60 µF +150-10% 25 V	4450-2900	56289	D17872	5910-799-9280
DIODES					
CR501 thru CR504	Type 1N1613	6081-1012	24446	1N1613	5960-764-3184
CR505 thru CR507	Type 1N4009	6082-1012	24446	1N4009	
CR508	Type 1N748A	6083-1002	07910	1N748A	5960-800-3973
CR551 thru CR554	Type 1N3253	6081-1001	79089	1N3253	5961-814-4251
CR559 thru CR563	Type 1N4009	6082-1012	24446	1N4009	
CR564	Type 1N957B	6083-1009	07910	1N957B	
TRANSISTORS					
Q501	Type 40251	8210-1097	12672	40251	
Q502	Type 2N697	8210-1040	82219	2N697	5961-752-0150
Q503	Type 2N3414	8210-1047	24446	2N3414	5961-989-2749
Q504	Type 2N3905	8210-1114	04713	2N3905	
Q505	Type 2N3905	8210-1114	04713	2N3905	
Q551	Type 2N3740	8210-1121		2N3740	
Q552	Type 2N3906	8210-1112	93916	2N3906	
Q553 thru Q554	Type 2N3414	8210-1047	24446	2N3414	5961-989-2749
Q555	Type 40250	8210-1095	12672	40250	
Q556	Type 2N3900	8210-1118	93916	2N3900	
Q557	Type 2N3638	8210-1096	07263	2N3638	
Q558	Type 2N3905	8210-1114	04713	2N3905	
RESISTORS					
R502	Potentiometer, Wire Wound, 500 Ω ±10%	6051-1509	02660	2600PC, 500 Ω ±10%	
R503	Composition, 2 kΩ ±5% 1/4 W	6099-2205	75042	BTS, 2 kΩ ±5%	5905-279-4029
R504	Composition, 56 Ω ±10% 1/4 W	6099-0569	75042	BTS, 56 Ω ±10%	
R505	Composition, 1 kΩ ±10% 1/4 W	6099-2109	75042	BTS, 1 kΩ ±10%	
R506	Composition, 47 Ω ±10% 1/4 W	6099-0479	75042	BTS, 47 Ω ±10%	
R507	Composition, 360 Ω ±5% 1/4 W	6099-1365	75042	BTS, 360 Ω ±5%	
R508	Wire Wound, 0.39 Ω ±5% 2 W	6761-9399	75042	BWH, 0.39 Ω ±5%	
R509	Composition, 47 Ω ±10% 1/4 W	6099-0479	75042	BTS, 47 Ω ±10%	
R510	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R511	Composition, 22 kΩ ±10% 1/4 W	6099-3229	75042	BTS, 22 kΩ ±10%	
R512	Composition, 12 kΩ ±10% 1/4 W	6099-3129	75042	BTS, 12 kΩ ±10%	
R513	Wire Wound, 0.39 Ω ±5% 2 W	6761-9399	75042	BWH, 0.39 Ω ±5%	
R551	Wire Wound, 2.7 Ω ±10% 2 W	6760-9279	75042	BWH, 2.7 Ω ±10%	5905-794-3857
R552	Composition, 3.9 Ω ±5% 1 W	6110-9395	01121	GB, 3.9 Ω ±5%	
R553	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R554	Composition, 10 Ω ±5% 1/4 W	6099-0105	75042	BTS, 10 Ω ±5%	5905-809-8596
R555	Wire Wound, 2.7 Ω ±10% 2 W	6760-9279	75042	BWH, 2.7 Ω ±10%	5905-794-3857
R556	Composition, 47 Ω ±5% 1/4 W	6099-0475	75042	BTS, 47 Ω ±5%	
R557	Film, 5.11 kΩ ±1% 1/8 W	6250-1511	75042	CEA, 5.11 kΩ ±1%	5905-577-6734
R559	Composition, 10 kΩ ±5% 1/4 W	6099-3105	75042	BTS, 10 kΩ ±5%	5905-683-2238
R560	Composition, 10 kΩ ±5% 1/4 W	6099-3105	75042	BTS, 10 kΩ ±5%	5905-683-2238
R561	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R562	Composition, 3.9 kΩ ±5% 1 W	6110-9395	01121	GB, 3.9 kΩ ±5%	
R563	Composition, 10 Ω ±5% 1/4 W	6099-0105	75042	BTS, 10 Ω ±5%	5905-809-8596
R564	Composition, 1.2 kΩ ±5% 1/4 W	6099-2125	75042	BTS, 1.2 kΩ ±5%	
R565	Composition, 47 Ω ±5% 1/4 W	6099-0475	75042	BTS, 47 Ω ±5%	
R566	Composition 82 kΩ ±5% 1/4 W	6099-3825	75042	BTS, 82 kΩ ±5%	
R567	Composition, 2.7 kΩ ±5% 1/4 W	6099-2275	75042	BTS, 2.7 kΩ ±5%	
R568	Composition 3 kΩ ±5% 1/4 W	6099-2305	75042	BTS, 3 kΩ ±5%	
R569	Potentiometer, Wire Wound, 1 kΩ ±10%	6051-2109	02660	2600-PC, 1 kΩ ±10%	
R570	Composition, 3.3 kΩ ±5% 1/4 W	6099-2335	75042	BTS, 3.3 kΩ ±5%	5905-681-9969
R571	Composition, 43 kΩ ±5% 1/4 W	6099-3435	75042	BTS, 43 kΩ ±5%	5905-549-9833
R572	Film, 5.11 kΩ ±1% 1/8 W	6250-1511	75042	CEA, 5.11 kΩ ±1%	5905-577-6734
R573	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
MISCELLANEOUS					
S501	Toggle	7910-1300	04009	83053-SA	5930-909-3510
S502	Slide	7910-0831	42190	4603	
F501	Fuse, 0.8 A	5330-1200	71400	MDL, 0.8 Amp	5920-284-6733
F502	Fuse, 0.4 A	5330-0900	71400	MDL, 0.4 Amp	5920-537-6654
PL501	Power Plug	4240-0600	24655	4240-0600	5935-816-0254
SO502	Socket	4230-2724	95354	91-6024-1201-00	

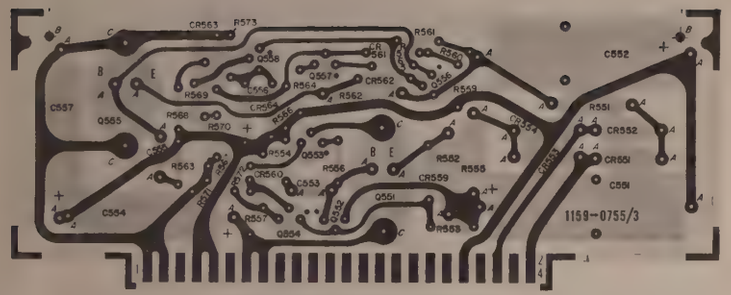


Figure 6-4A. ±15-V Power Supply, P/N 1159-4756.

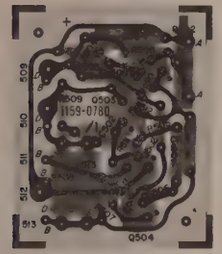


Figure 6-4B. 5-V Power Supply, P/N 1159-2781.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

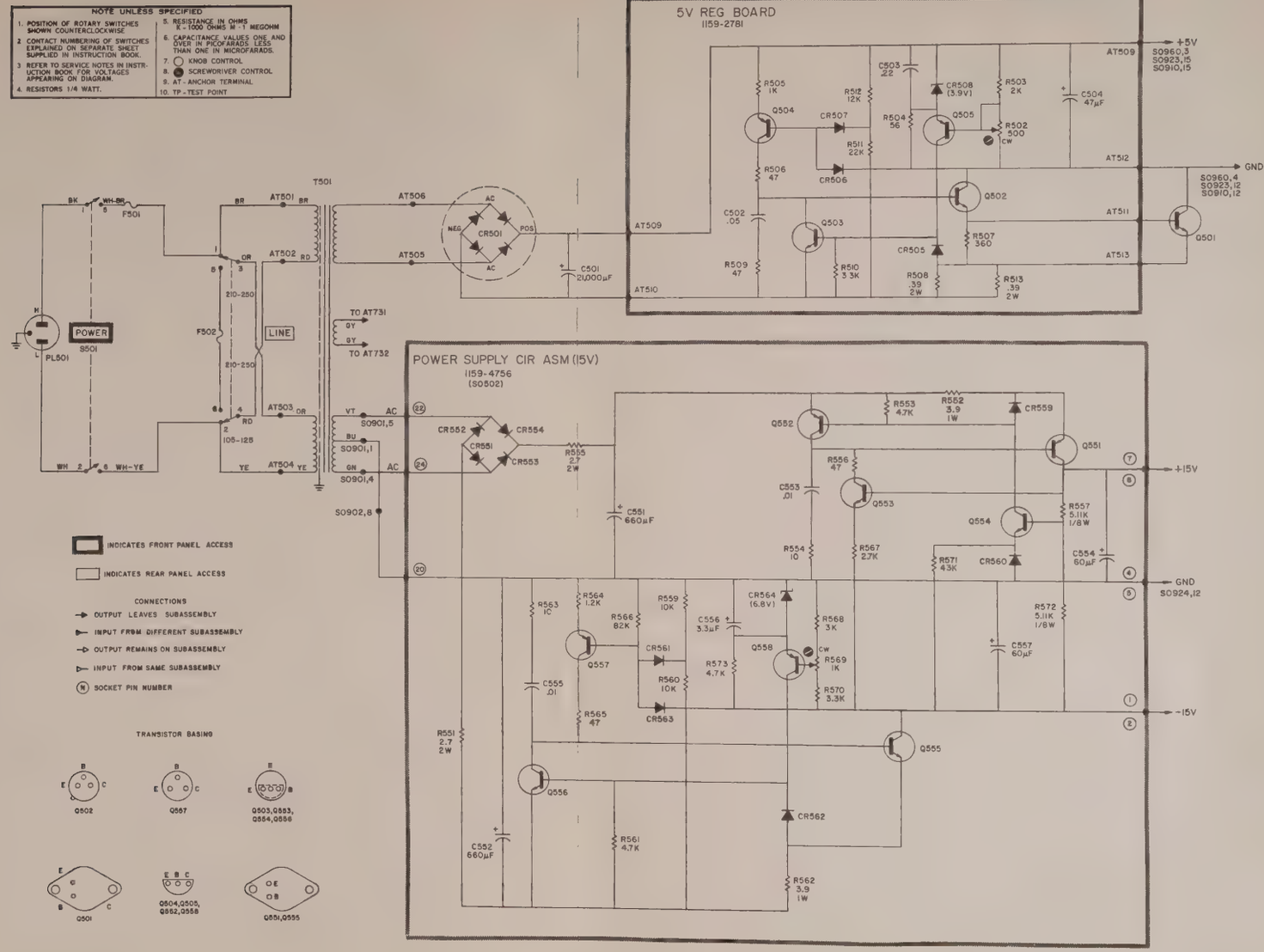


Figure 6-4. Power Supplies.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg Part No.	Fed. Stock No.
CAPACITORS					
C601	Mica, 75 pF ±5%	4700-0375	14655	22A, 75 pF ±5%	
C602	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C603	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C604	Ceramic, 20 pF ±10% 500 V	4404-0208	72982	831, 20 pF ±10%	
C605	Ceramic, 0.1 µF	4400-2050	80183	5C13, 0.1 µF ±20%	5910-974-5695
C606	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C607	Ceramic, 100 pF ±10% 500 V	4404-1108	72982	831, 100 pF ±10%	
C608	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C609	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C610	Ceramic, 68 pF ±10% 500 V	4404-0688	72982	831, 68 pF ±10%	
C611	Ceramic, 100 pF ±10% 500 V	4404-1108	72982	831, 100 pF ±10%	
C612	Ceramic, 82 pF ±10% 500 V	4404-0828	72982	831, 82 pF ±10%	
C613	Ceramic, 0.0015 µF ±10% 500 V	4406-2158	72982	811, 0.0015 µF ±10%	
C614	Ceramic, 0.0015 µF ±10% 500 V	4406-2158	72982	811, 0.0015 µF ±10%	
C615	Ceramic, 470 pF ±10% 500 V	4404-1478	72982	831, 470 pF ±10%	
C616	Ceramic, 68 pF ±5% 500 V	4404-0685	72982	831, 68 pF ±5%	
C617	Ceramic, 47 pF ±5% 500 V	4404-0475	72982	831, 47 pF ±5%	
C618	Ceramic, 68 pF ±10% 500 V	4404-0688	72982	831, 68 pF ±10%	
C619	Electrolytic, 47Ω ±20% 6 V	4450-5500	56289	150D476X0006B2	5910-752-4185
C620	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C621	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C622	Ceramic, 0.001 µF ±10% 500 V	4405-2108	72982	801, 0.001 µF ±10%	
C651	Composition, 0.01 µF +80-20% 50 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
DIODES					
CR601	Type 1N758A	6083-1012	07910	1N758-A	
CR602	Type M1838	6084-1021	04713	MY838	
CR603	Type 1N4009	6082-1012	24446	1N4009	
CR604	Type 1N4009	6082-1012	24446	1N4009	
CR605	Type 1N995	6082-1002	80368	1N995	
CR606 thru CR609	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR610	Type 1N995	6082-1002	80368	1N995	
CR611	Type 1N4009	6082-1012	24446	1N4009	
CR612	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR613	Type 1N4009	6082-1012	24446	1N4009	
CR614	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR615	Type 1N4009	6082-1012	24446	1N4009	
CR616	Type 1N4009	6082-1012	24446	1N4009	
CR617	Type 1N995	6082-1002	80368	1N995	
INTEGRATED CIRCUITS					
IC601		5431-9603	93332	SG83-03	
IC602		5431-8190	01295	SN7490N	
IC603		5431-8190	01295	SN7490N	
IC604		5431-8200	01295	SN74H00N	
IC605		5431-9462	07263	DTµL-946	
IC606		5431-8176	01295	SN7476N	
IC607		5431-8210	01295	SN74H10N	
IC608		5431-8240	01295	SN74H40N	
INDUCTOR					
L601		1399-2600	24655	1399-2600	
RESISTORS					
R601	Composition, 240 Ω ±5% 1/4 W	6099-1245	75042	BTS, 240 Ω ±5%	
R602	Composition 10 kΩ ±5% 1/4 W	6099-3105	75042	BTS, 10 kΩ ±5%	5905-683-2238
R603	Composition 18 kΩ ±5% 1/4 W	6099-3185	75042	BTS, 18 kΩ ±5%	5905-687-0000
R604	Composition, 1 kΩ ±5% 1/4 W	6099-2105	75042	BTS, 1 kΩ ±5%	5905-681-6462
R605	Composition 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R606	Composition, 1 kΩ ±5% 1/4 W	6099-2105	75042	BTS, 1 kΩ ±5%	5905-681-6462
R607	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R608	Composition, 100 Ω ±5% 1/4 W	6099-1105	75042	BTS, 100 Ω ±5%	
R609	Composition 10 Ω ±5% 1/4 W	6099-0105	75042	BTS, 10 Ω ±5%	5905-809-8596
R610	Composition, 2.2 kΩ ±5% 1/4 W	6099-2225	75042	BTS, 2.2 kΩ ±5%	5905-723-5251
R612	Composition, 1 kΩ ±10% 1/4 W	6099-2109	75042	BTS, 1 kΩ ±10%	
R613	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R614	Composition, 1 kΩ ±10% 1/4 W	6099-2109	75042	BTS, 1 kΩ ±10%	
R615	Composition, 22 kΩ ±10% 1/4 W	6099-3229	75042	BTS, 22 kΩ ±10%	
R616	Composition, 2.7 k ±10% 1/4 W	6099-2279	75042	BTS, 2.7 kΩ ±10%	
R617	Composition, 220 kΩ ±10% 1/4 W	6099-4229	75042	BTS, 220 kΩ ±10%	
R618	Composition, 10 kΩ ±10% 1/4 W	6099-3109	75042	BTS, 10 kΩ ±10%	
R619	Composition, 18 kΩ ±5% 1/4 W	6099-3185	75042	BTS, 18 kΩ ±5%	5905-687-0000
R620	Composition, 10 kΩ ±5% 1/4 W	6099-3105	75042	BTS, 10 kΩ ±5%	5905-683-2238
R621	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R622	Composition, 4.7 kΩ ±10% 1/4 W	6099-2479	75042	BTS, 4.7 kΩ ±10%	
R623	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R624	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R625	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R626	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R627	Composition, 680 Ω ±10% 1/4 W	6099-1689	75042	BTS, 680 Ω ±10%	
R628	Composition, 3.9 kΩ ±10% 1/4 W	6099-2399	75042	BTS, 3.9 kΩ ±10%	
R629	Composition, 3.9 kΩ ±10% 1/4 W	6099-2399	75042	BTS, 3.9 kΩ ±10%	

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
RESISTORS (Cont)					
R630	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R631	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R632	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R633	Composition, 22 kΩ ±10% 1/4 W	6099-3229	75042	BTS, 22 kΩ ±10%	
R634	Composition, 6.8 kΩ ±10% 1/4 W	6099-2689	75042	BTS, 6.8 kΩ ±10%	
R635	Composition, 27 kΩ ±10% 1/4 W	6099-3279	75042	BTS, 27 kΩ ±10%	
R636	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R637	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R638	Composition, 10 kΩ ±10% 1/4 W	6099-3109	75042	BTS, 10 kΩ ±10%	
R639	Composition, 1 kΩ ±10% 1/4 W	6099-2109	75042	BTS, 1 kΩ ±10%	
R640	Composition, 560 Ω ±5% 1/4 W	6099-1565	75042	BTS, 560 Ω ±5%	
R641	Composition, 560 Ω ±5% 1/4 W	6099-1565	75042	BTS, 560 Ω ±5%	
R651	Film, 20 kΩ ±1% 1/8 W	6250-2200	75042	CEA, 20 kΩ ±1%	5905-702-5971
R652	Composition, 4.7 kΩ ±5% 1/2 W	6100-2475	01121	RC20GF472J	5905-279-3504
R653	Composition, 6.2 kΩ ±5% 1/2 W	6100-2625	01121	RC20GF622J	5905-279-2673
R654	Film, 20 kΩ ±1% 1/8 W	6250-2200	75042	CEA, 20 kΩ ±1%	5905-702-5971
R655	Precision, 10 kΩ ±1% .30 W	6730-2100	80131	A22, 10 kΩ ±1%	
R656	Composition, 1.5 kΩ ±5% 1/2 W	6100-2155	01121	RC20GF152J	5905-841-7461
R657	Composition, 10 k ±5% 1/2 W	6100-3105	01121	RC20GF103J	5905-185-8510
R658	Composition, 1.0 MΩ ±5% 1/2 W	6100-5105	01121	RC20GF105J	5905-192-0390
TRANSISTORS					
Q601	Type 2N3563	8210-1066	07263	2N3563	
Q602	Type 2N3563	8210-1066	07263	2N3563	
Q603	Type 2N4275	8210-1126	23342	2N4275	
Q604	Type 2N4125	8210-1125	93916	2N4125	
Q605	Type 2N4275	8210-1126	23342	2N4275	
Q651	Type 2N3900	8210-1118	93916	2N3900	
Q652	Type 2N3900	8210-1118	93916	2N3900	
Q653	Type 2N3906	8210-1112	93916	2N3906	
Q654	Type 2N697	8210-1040	82219	2N697	5961-752-0150

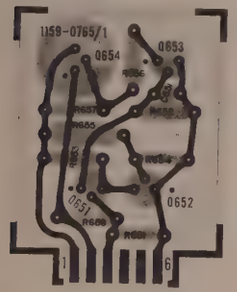
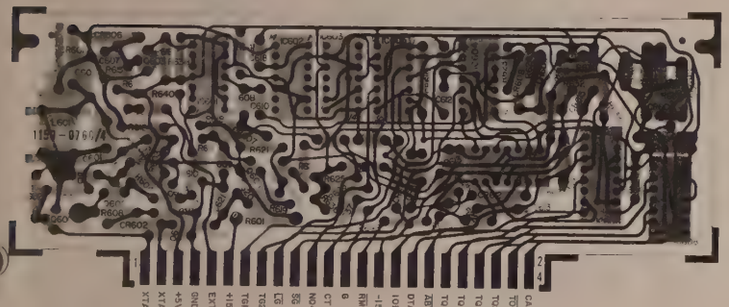


Figure 6-5A. Oven Control, P/N 1159-4765.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

Figure 6-5B. Clock, P/N 1159-4760.



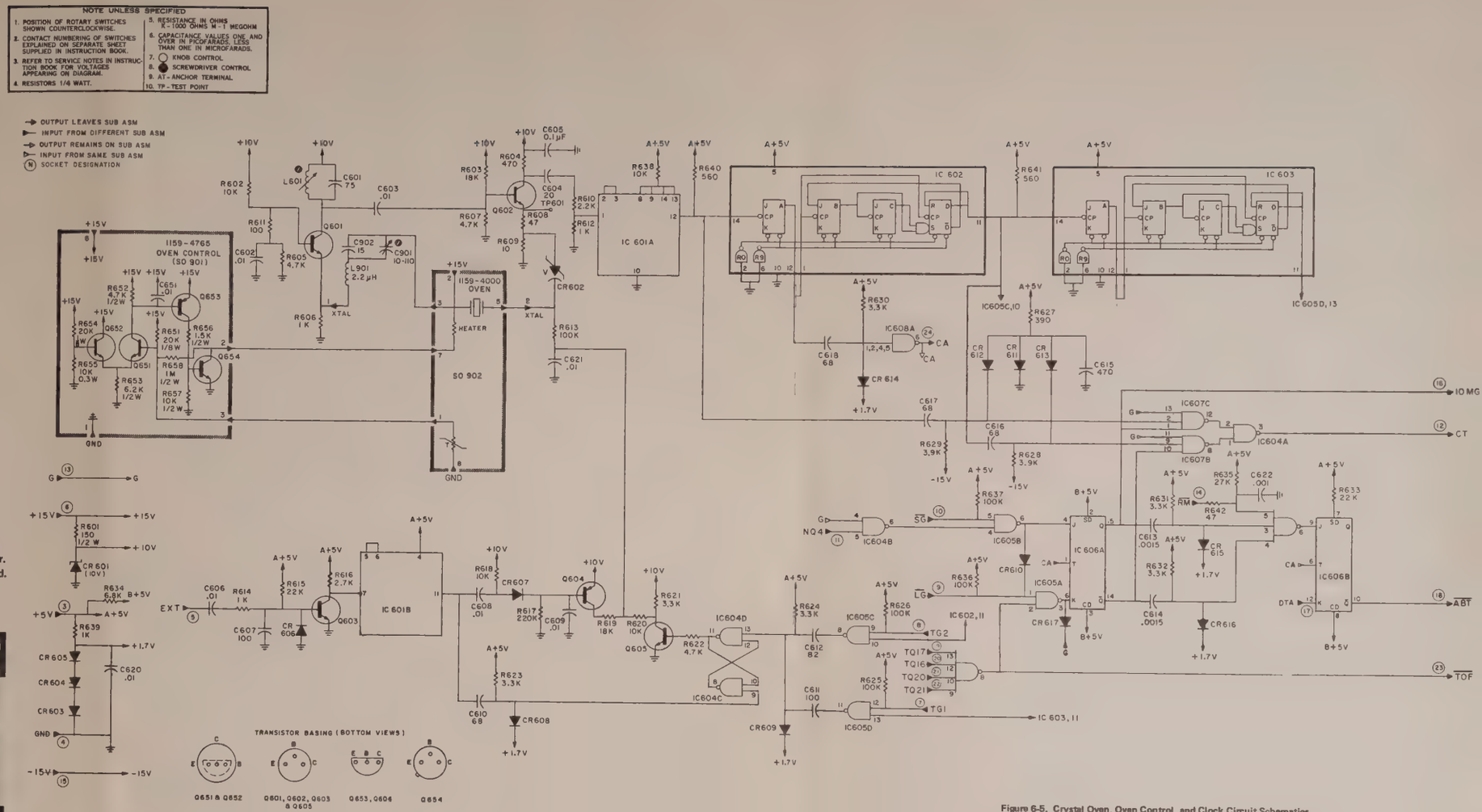


Figure 6-5. Crystal Oven, Oven Control, and Clock Circuit Schematics.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C101	Plastic, 0.1 µF ±10% 200 V	4860-8253	84411	663UW, 0.1 µF ±10%	
C102	Ceramic, 3.3 pF ±10% 500 V	4400-0400	78488	GA, 3.3 pF ±10%	
C103	Ceramic, 2.2 µF ±20% 25 V	4400-2080	80183	5C13, 2.2 µF ±20%	
C104	Ceramic, 0.1 µF ±20% 25 V	4400-2050	80183	5C13, 0.1 µF ±20%	5910-974-5695
C105	Ceramic, 0.001 µF ±5% 500 V	4405-2105	72982	801, 0.001 µF ±5%	
C106	Ceramic, 2.2 µF ±20% 25 V	4400-2080	80183	5C13, 2.2 µF ±20%	
C107	Ceramic, 0.01 µF ±20% 500 V	4406-3100	72982	811, 0.01 µF ±20%	
C108	Ceramic, 100 pF ±5% 500 V	4404-1105	72982	831, 100 pF ±5%	
C109	Ceramic, 0.1 µF ±20% 25 V	4400-2050	80183	5C13, 0.1 µF ±20%	5910-974-5695
C110	Ceramic, 47 pF ±10% 500 V	4404-0478	72982	831, 47 pF ±10%	
C111	Ceramic, 47 pF ±10% 500 V	4404-0478	72982	831, 47 pF ±10%	
C112	Ceramic, 0.01 µF +80-20% 50 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C113	Ceramic, 0.01 µF +80-20% 50 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C114	Ceramic, 1.0 µF ±20% 35 V	4450-4300	56289	150D105X0035A2	5910-726-5003
C115	Ceramic, 1.8 pF ±5% 500 V	4400-0180	78488	GA, 1.8 pF ±5%	
C116	Ceramic, 15 pF ±10% 500 V	4404-0158	72982	831, 15 pF ±10%	
C117	Ceramic, 15 pF ±10% 500 V	4404-0158	72982	831, 15 pF ±10%	
C118	Ceramic, 1.0 µF ±20% 35 V	4450-4300	56289	150D105X0035A2	5910-726-5003
C119	Ceramic, 0.01 µF +80-20% 50 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C120	Ceramic, 2.2 µF ±20% 25 V	4400-2080	80183	5C13, 2.2 µF ±20%	
C121	Ceramic, 2.2 µF ±20% 25 V	4400-2080	80183	5C13, 2.2 µF ±20%	
INTEGRATED CIRCUITS					
IC101		5431-9362	07263	DTµL 936	
IC102		5431-8200	01295	SN74H00N	
DIODES					
CR101 thru CR104	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR105	Type 1N750A	6083-1028	07910	1N750A	5960-754-5897
CR106 thru CR109	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR110	Type 1N750A	6083-1028	07910	1N750A	5960-754-5897
CR111 thru CR114	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR115	Type 1N750A	6083-1028	07910	1N750A	5960-754-5897
CR116 thru CR121	Type 1N4009	6082-1012	24446	1N4009	
CR122 thru CR123	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
RESISTORS					
R101	Composition, 2.0 MΩ ±5% 1/4 W	6099-5205	75042	BTS, 2.0 MΩ ±5%	
R102 thru R103	Composition 1.0 MΩ ±5% 1/4 W	6099-5105	75042	BTS, 1.0 MΩ ±5%	
R104	Composition, 2.7 kΩ ±5% 1/4 W	6099-2275	75042	BTS, 2.7 kΩ ±5%	
R105	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R106	Composition, 7.5 kΩ ±5% 1/4 W	6099-2755	75042	BTS, 7.5 kΩ ±5%	
R107	Composition, 1.2 kΩ ±5% 1/4 W	6099-2125	75042	BTS, 1.2 kΩ ±5%	
R108	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R109	Composition, 680Ω ±10% 1/4 W	6099-1689	75042	BTS, 680Ω ±10%	
R110 thru R111	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R112	Composition, 680 Ω ±10% 1/4 W	6099-1689	75042	BTS, 680 Ω ±10%	
R113	Composition, 1.0 MΩ ±5% 1/4 W	6099-5105	75042	BTS, 1.0 MΩ ±5%	
R114	Composition, 2.7 kΩ ±5% 1/4 W	6099-2275	75042	BTS, 2.7 kΩ ±5%	
R115	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R116	Composition, 7.5 kΩ ±5% 1/4 W	6099-2755	75042	BTS, 7.5 kΩ ±5%	
R117	Composition, 1.2 kΩ ±5% 1/4 W	6099-2125	75042	BTS, 1.2 kΩ ±5%	
R118	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R119	Composition, 680 Ω ±10% 1/4 W	6099-1689	75042	BTS, 680 Ω ±10%	
R120 thru R122	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R123	Composition, 680 Ω ±10% 1/4 W	6099-1689	75042	BTS, 680 Ω ±10%	
R124	Composition, 1.0 MΩ ±5% 1/4 W	6099-5105	75042	BTS, 1.0 MΩ ±5%	
R125	Potentiometer, 5 kΩ ±10%	6051-2509	80294	3007P-1-502	
R126	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R127	Composition, 7.5 kΩ ±5% 1/4 W	6099-2755	75042	BTS, 7.5 kΩ ±5%	
R128 thru R129	Composition, 1.2 kΩ ±5% 1/4 W	6099-2125	75042	BTS, 1.2 kΩ ±5%	
R130	Composition, 100 Ω ±5% 1/4 W	6099-1105	75042	BTS, 100 Ω ±5%	
R131	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R132	Composition, 2.7 kΩ ±5% 1/4 W	6099-2275	75042	BTS, 2.7 kΩ ±5%	
R133	Composition, 1.5 kΩ ±5% 1/4 W	6099-2155	75042	BTS, 1.5 kΩ ±5%	
R134 thru R135	Composition, 100 Ω ±5% 1/4 W	6099-1105	75042	BTS, 100 Ω ±5%	

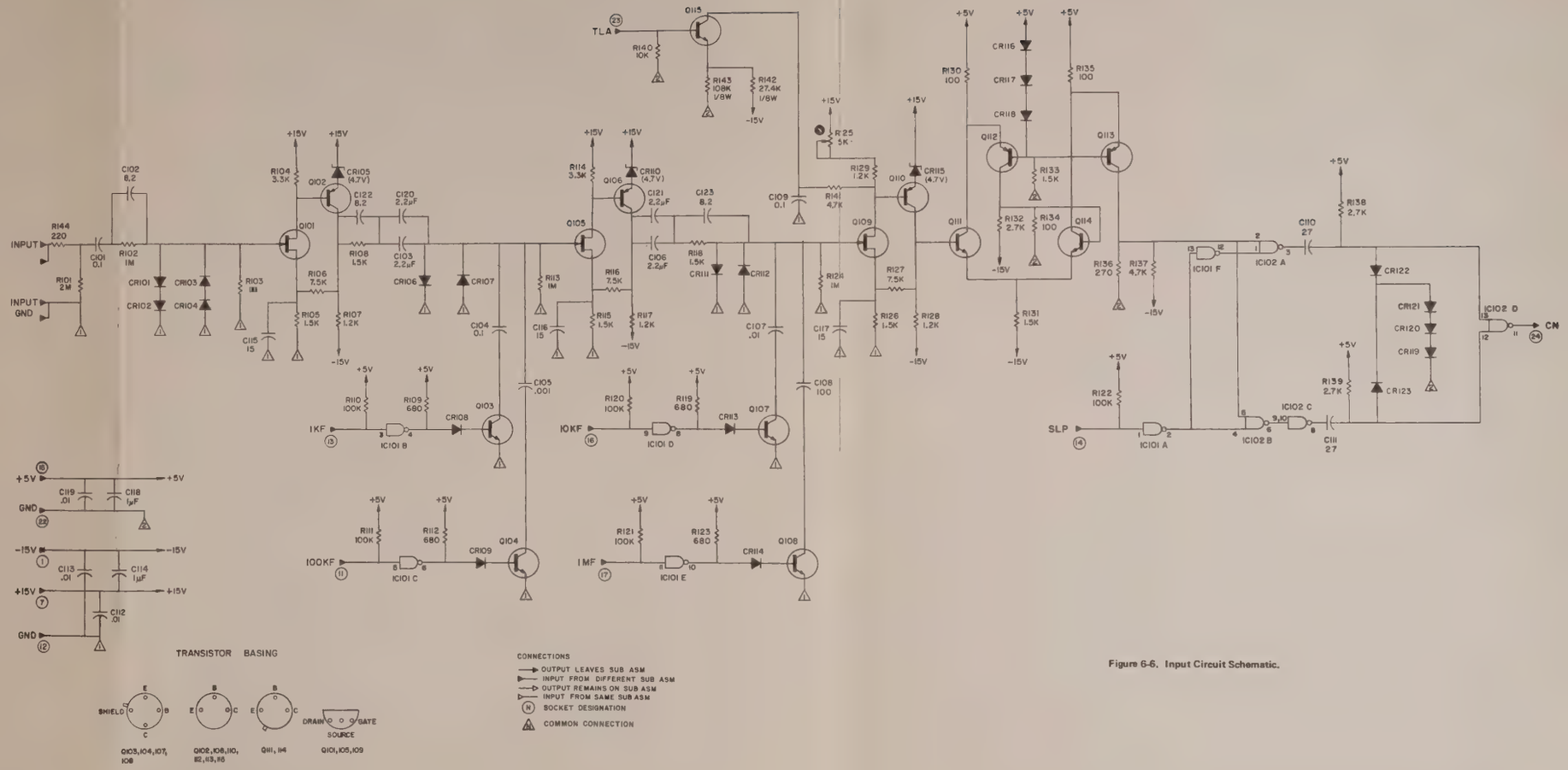
Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
RESISTORS (Cont)					
R136	Composition, 270 Ω ±5% 1/4 W	6099-1275	75042	BTS, 270 Ω ±5%	
R137	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R138 thru R139	Composition, 2.7 kΩ ±5% 1/4 W	6099-2275	75042	BTS, 2.7 kΩ ±5%	
R140	Composition, 10 kΩ ±5% 1/4 W	6099-3105	75042	BTS, 10 kΩ ±5%	5905-683-2238
R141	Composition, 4.7 kΩ ±5% 1/4 W	6099-2475	75042	BTS, 4.7 kΩ ±5%	5905-686-9998
R142	Film, 27.4 kΩ ±1% 1/8 W	6250-2274	75042	CEA, 27.4 kΩ ±1%	
R143	Film, 108 kΩ ±1% 1/8 W	6250-3108	75042	CEA, 108 kΩ ±1%	
TRANSISTORS					
Q101	Type MPF102	8210-1150	93916	MPF102	
Q102	Type 2N4121	8210-1151	93916	2N4121	
Q103	Type 2N3933	8210-1122	93916	2N3933	
Q104	Type 2N3933	8210-1122	93916	2N3933	
Q105	Type MPF102	8210-1150	93916	MPF102	
Q106	Type 2N4121	8210-1151	93916	2N4121	
Q107	Type 2N3933	8210-1122	93916	2N3933	
Q108	Type 2N3933	8210-1122	93916	2N3933	
Q109	Type MPF102	8210-1150	93916	MPF102	
Q110	Type 2N4121	8210-1151	93916	2N4121	
Q111	Type 2N709	8210-1054	75491	2N709	5960-995-7824
Q112	Type 2N4258	8210-1136	93916	2N4258	
Q113	Type 2N4258	8210-1136	93916	2N4258	
Q114	Type 2N709	8210-1054	75491	2N709	5960-995-7824
Q115	Type SE4010	8210-1139	93916	SE4010	

Figure 6-6. Input, P/N 1159-4711.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

NOTE UNLESS SPECIFIED

1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE.
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK.
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM.
4. RESISTORS 1/4 WATT.
5. RESISTANCE IN OHMS K - 1000 OHMS M - 1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN PICOFARADS. LESS THAN ONE IN MICROFARADS
7. KNOB CONTROL
8. SCREWDRIVER CONTROL
9. AT - ANCHOR TERMINAL
10. TP - TEST POINT



TRANSISTOR BASING

CONNECTIONS

- OUTPUT LEAVES SUB ASM
- INPUT FROM DIFFERENT SUB ASM
- OUTPUT REMAINS ON SUB ASM
- INPUT FROM SAME SUB ASM
- (N) SOCKET DESIGNATION
- COMMON CONNECTION

Figure 6-6. Input Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C151	Ceramic, 0.0047 µF ±20%	4405-2470	72982	801, 0.0047 µF ±20%	
C152	Electrolytic, 68 µF ±10% 6 V	4450-5851	80183	109D686X9006C2	
C153	Ceramic, 470 pF ±10% 500 V	4404-1478	72982	831, 470 pF ±10%	
INTEGRATED CIRCUITS					
IC151		5431-9462	07263	DTµL-946	
IC152		5431-9462	07263	DTµL-946	
IC153		5431-9622	07263	DTµL-962	
IC154		5431-9462	07263	DTµL-946	
IC155		5431-9362	07263	DTµL-936	
IC156		5431-8200	01295	SN74H00N	
IC157		5431-8272	01295	SN74H72N	
IC158		5431-8200	01295	SN74H00N	
RESISTORS					
R151	Composition, 180 Ω ±10% 1/4 W	6099-1189	75042	BTS, 180 Ω ±10%	
R152	Composition, 820 Ω ±10% 1/4 W	6099-1829	75042	BTS, 820 Ω ±10%	
R153	Composition, 150 kΩ ±10% 1/4 W	6099-4159	75042	BTS, 150 kΩ ±10%	
R154	Composition, 15 Ω ±10% 1/4 W	6099-0159	75042	BTS, 15 Ω ±10%	
R155	Composition, 3.9 kΩ ±5% 1/4 W	6099-2395	75042	BTS, 3.9 kΩ ±5%	
R156	Composition, 330 Ω ±10% 1/4 W	6099-1339	75042	BTS, 330 Ω ±10%	
R157	Composition, 5.6 kΩ ±10% 1/4 W	6099-2569	75042	BTS, 5.6 kΩ ±10%	
R158	Composition, 470 kΩ ±5% 1/4 W	6099-4475	75042	BTS, 470 kΩ ±5%	
R159	Composition, 47 kΩ, ±10% 1/4 W	6099-3479	75042	BTS, 47 kΩ ±10%	
R160	Composition, 47 kΩ ±10% 1/4 W	6099-3479	75042	BTS, 47 kΩ ±10%	
TRANSISTORS					
Q151	Type 2N3638	8210-1096	07263	2N3638	
Q152	Type 2N3414	8210-1047	24446	2N3414	5961-989-2749
Q153	Type 2N3414	8210-1047	24446	2N3414	5961-989-2749
Q154	Type 2N3414	8210-1047	24446	2N3414	5961-989-2749

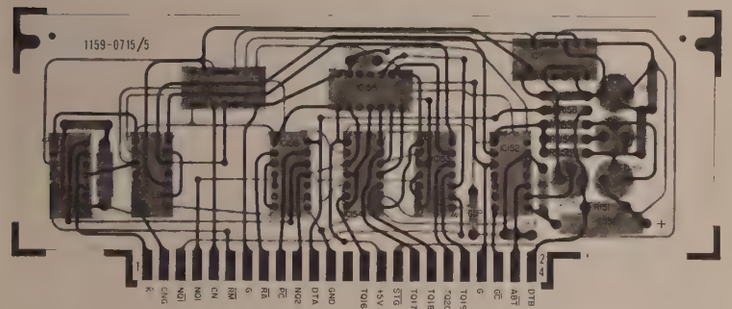


Figure 6-7. Gate, P/N 1159-4715

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

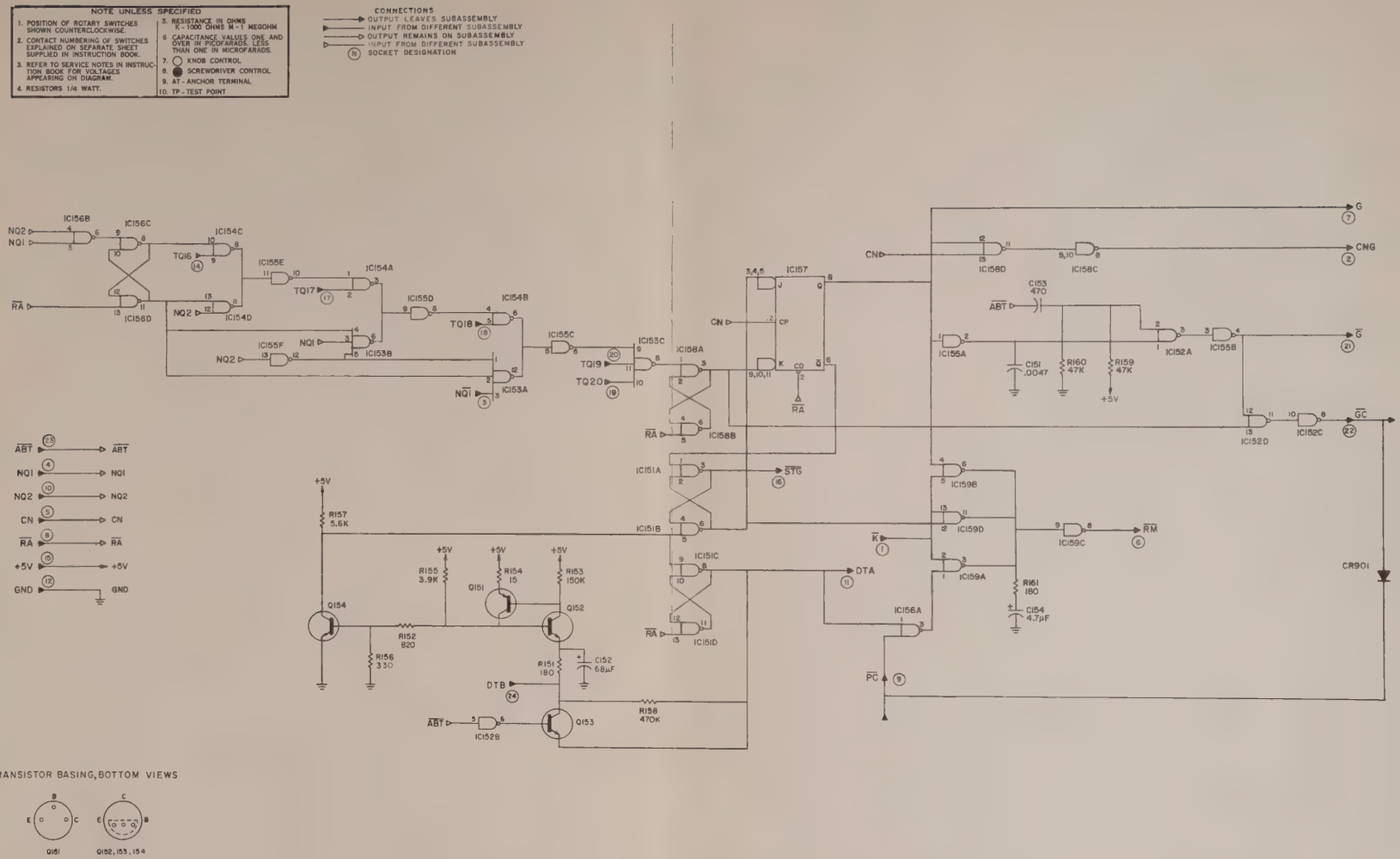


Figure 6-7. Gate Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C201 thru C212	Composition, 47 pF ±10% 500 V	4404-0478	72982	831, 47 pF ±10%	
C213	Composition, 0.001 pF ±10% 500 V	4405-2108	72982	801, 0.001 pF ±10%	
C214	Composition, 0.01 μF +80-20% 500 V	4404-3100	72982	831, 0.01 μF +80-20%	
INTEGRATED CIRCUITS					
IC201 thru IC212		5431-8271	01295	SN74H71N	
IC213 thru IC214		5431-8140	01295	SN7440N	
RESISTORS					
R201 thru R211	Composition, 6.8 kΩ ±10% 1/4 W	6099-2689	75042	BTS, 6.8 kΩ ±10%	
R212 thru R214	Composition, 4.7 kΩ ±10% 1/4 W	6099-2479	75042	BTS, 4.7 kΩ ±10%	
R213 thru R214	Composition, 680 Ω ±10% 1/4 W	6099-1689	75042	BTS, 680 Ω ±10%	
DIODES					
CR201 thru CR212	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR213 thru CR216	Type 1N4009	6082-1012	24446	1N4009	
TRANSISTOR					
Q201	Type 2N4275	8210-1126	23342	2N4275	

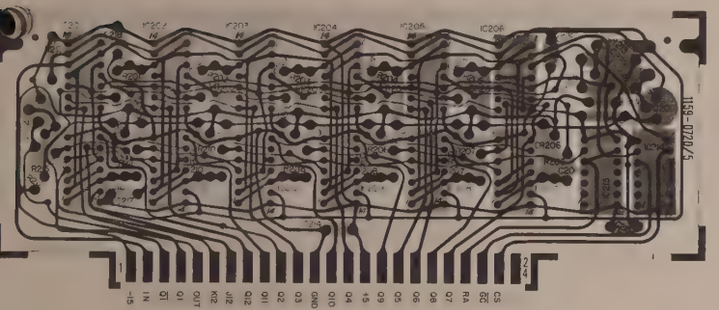
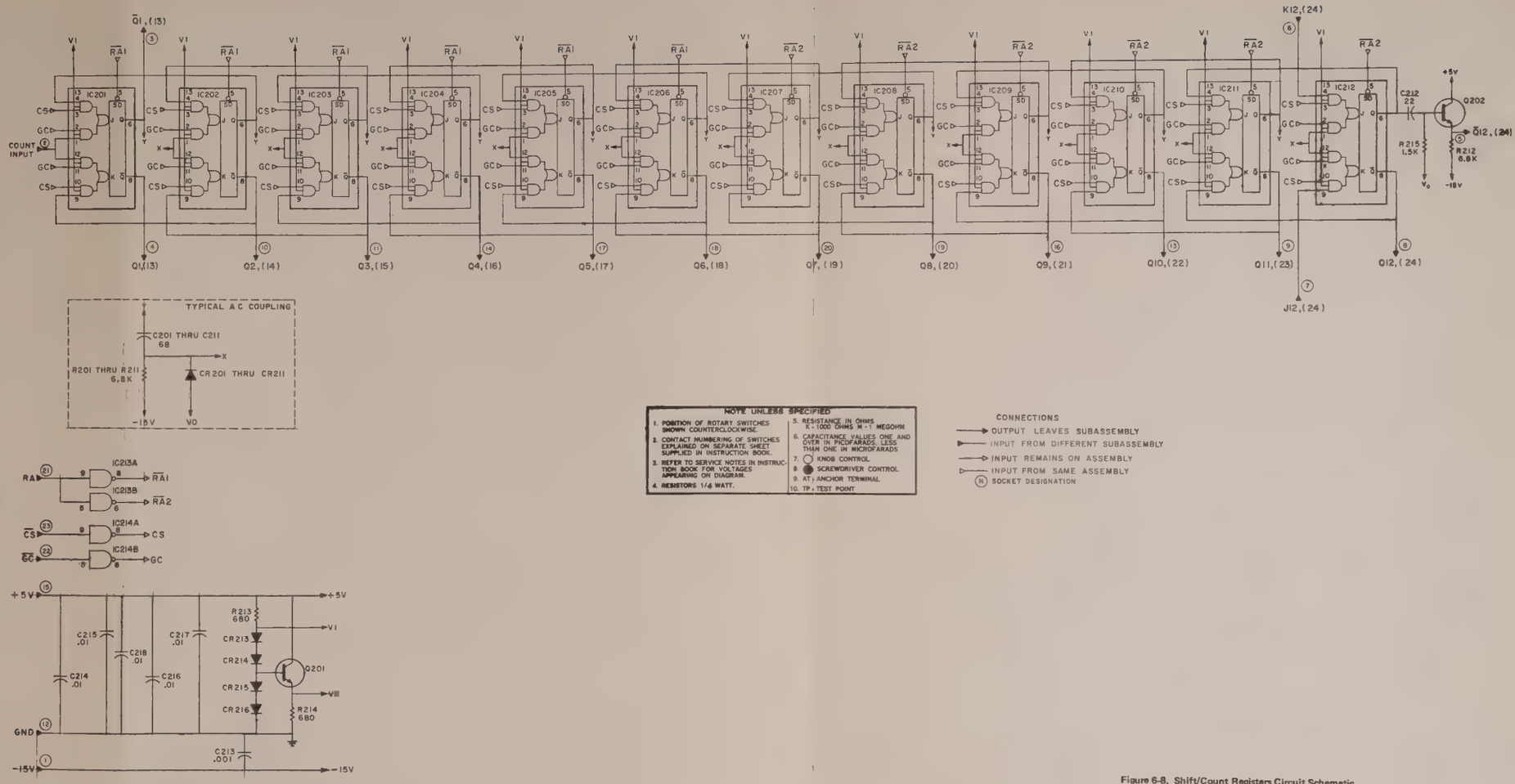


Figure 6-8. Shift/Count Registers, P/N 1159-4720.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.



NOTE UNLESS SPECIFIED

1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE.
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK.
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM.
4. RESISTORS 1/4 WATT.
5. RESISTANCE IN OHMS K=1000 OHMS M=1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN MICROFARADS, LESS THAN ONE IN MICROFARADS
7. KNOB CONTROL
8. SCREWDRIVER CONTROL
9. AT ANCHOR TERMINAL
10. TP TEST POINT

CONNECTIONS

- OUTPUT LEAVES SUBASSEMBLY
- INPUT FROM DIFFERENT SUBASSEMBLY
- INPUT REMAINS ON ASSEMBLY
- INPUT FROM SAME ASSEMBLY
- (N) SOCKET DESIGNATION

Figure 6-8. Shift/Count Registers Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
INTEGRATED CIRCUITS					
IC401					
thru		5431-8253	01295	SN74H53N	
IC404					
IC405		5431-8200	01295	SN74H00N	
IC406					
thru		5431-8176	01295	SN7476N	
IC409					
IC410		5431-8211	01295	SN74H11N	
RESISTORS					
R401					
thru	Composition, 10 kΩ ±10% 1/4 W	6099-3109	75042	BTS, 10 kΩ ±10%	
R402					
R403	Composition, 6.8 kΩ ±10% 1/4 W	6099-2689	75042	BTS, 6.8 kΩ ±10%	
R404	Composition, 12 kΩ ±10% 1/4 W	6099-3129	75042	BTS, 12 kΩ ±10%	

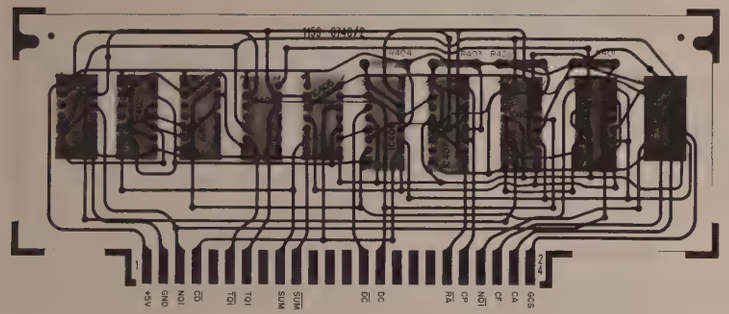


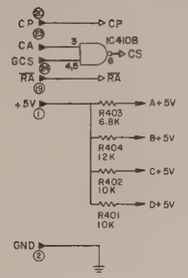
Figure 6-9. Arithmetic Program, P/N 1159-4740.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

NOTE UNLESS SPECIFIED

1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE.
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK.
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM.
4. RESISTORS 1/4 WATT.
5. RESISTANCE IN OHMS K - 1000 OHMS M - 1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN PICOFARADS, LESS THAN ONE IN MICROFARADS
7. KNOB CONTROL
8. SCREWDRIVER CONTROL
9. AT - ANCHOR TERMINAL
10. TP - TEST POINT

OUTPUT LEAVES SUBASSEMBLY
INPUT FROM DIFFERENT SUBASSEMBLY
OUTPUT REMAINS ON SUBASSEMBLY
INPUT FROM SAME SUBASSEMBLY
(N) SOCKET PIN NUMBER



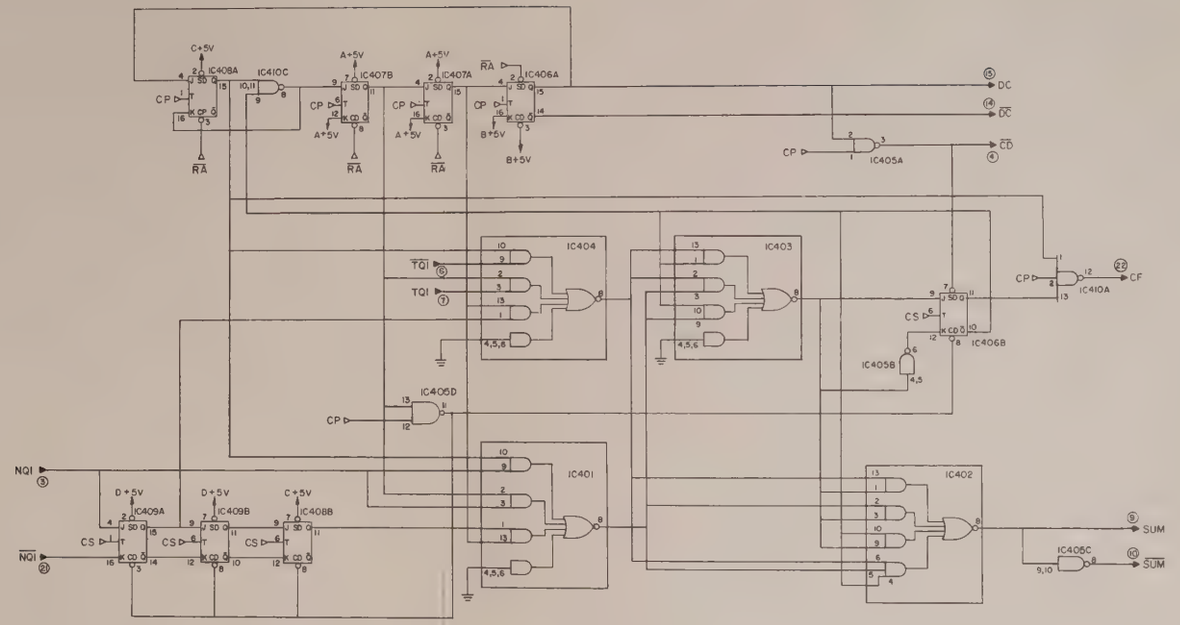


Figure 6-9. Arithmetic Program Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C251 thru C253	Ceramic, 100 pF ±10% 500 V	4404-1108	72982	831, 100 pF ±10%	
C301 thru C303	Ceramic, 100 pF ±10% 500 V	4404-1108	72982	831, 100 pF ±10%	
C701 thru C702	Electrolytic, 4 μF +150-10% 300 V	4450-3200	37942	TCW-20-41605	5910-962-0491
DIODES					
CR251 thru CR253	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR254 thru CR256	Type 1N4009	6082-1012	24446	1N4009	
CR301 thru CR303	Type 1N4009	6082-1012	24446	1N4009	
CR304 thru CR306	Type 1N3604	6082-1001	24446	1N3604	5960-995-2199
CR701 thru CR706	Type 1N645	6082-1016	24446	1N645	5961-944-8222
CR707 thru CR710	Type 1N3254	6081-1002	09213	1N3254	5961-082-3988
CR711	Type 1N645	6082-1016	24446	1N645	5961-944-8222
CR712	Type 1N4009	6082-1012	24446	1N4009	
INTEGRATED CIRCUITS					
IC251 thru IC253		5431-8190	01295	SN7490N	
IC254		5431-8176	01295	SN7476N	
IC255 thru IC256		5431-8100	01295	SN7400N	
IC257		5431-9302	07263	DTμL-930	
IC258 thru IC259		5431-9362	07263	DTμL-936	
IC260		5431-9322	07263	DTμL-932	
IC301		5431-8176	01295	SN7476N	
IC302		5431-8190	01295	SN7490N	
IC303		5431-8100	01295	SN7400N	
IC304		5431-8190	01295	SN7490N	
IC305		5491-9362	07263	DTμL-936	
IC306		5431-8190	01295	SN7490N	
IC307		5431-9362	07263	DTμL-936	
IC308		5431-8176	01295	SN7476N	
IC309		5431-8190	01295	SN7490N	
IC310		5431-8100	01295	SN7400N	
IC701 thru IC706	Digital	5431-9602	07263	CUL960	
RESISTORS					
R251 thru R253	Composition, 3.9 kΩ ±10% 1/4 W	6099-2399	75042	BTS, 3.9 kΩ ±10%	
R254	Composition, 1.5 kΩ ±10% 1/4 W	6099-2159	75042	BTS, 1.5 kΩ ±10%	
R301	Composition, 1.5 kΩ ±10% 1/4 W	6099-2159	75042	BTS, 1.5 kΩ ±10%	
R302 thru R304	Composition, 3.7 kΩ ±10% 1/4 W	6099-2399	75042	BTS, 3.9 kΩ ±10%	
R701 thru R706	Composition, 30 kΩ ±5% 1 W	6110-3305	01121	RC32GF303J	5905-299-2017
R707 thru R730	Composition, 1 kΩ ±10% 1/4 W	6099-2109	75042	BTS, 1 kΩ ±10%	
R731	Composition, 15 Ω ±5% 1/2 W	6100-0155	01121	RC20GF150J	5905-279-3521
R733	Precision, 5.1 kΩ ±5% 3 W	6680-2515	80183	242E, 5.1 kΩ ±5%	
R735	Composition, 2.2 kΩ ±10% 1/4 W	6099-2229	75042	BTS, 2.2 kΩ ±10%	
TUBES					
V701 thru V706	Tube, Digital Indicator	5437-0845	83781	NL-845	
SOCKETS					
SO701 thru SO706	Socket	7540-3465	83781	RTS-12	
TRANSISTORS					
Q701	Type 2N3440	8210-1098	04713	2N7440	

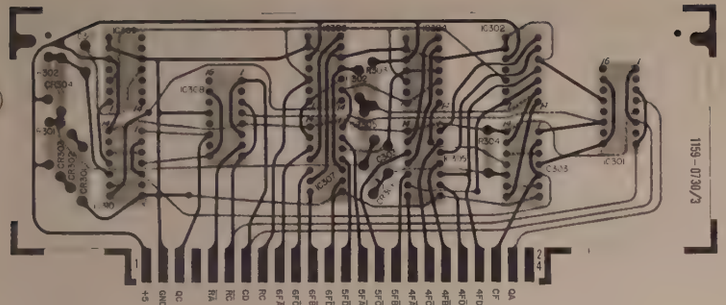


Figure 6-10A. Quotient Register A, P/N 1159-4725.

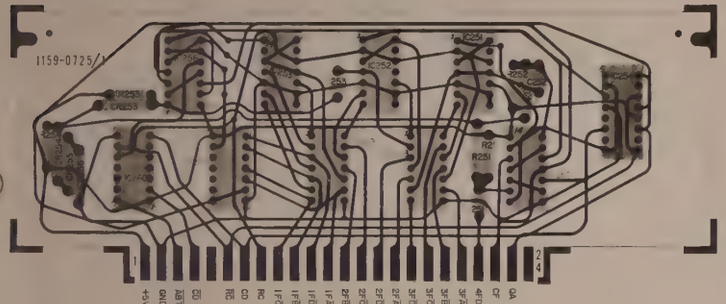


Figure 6-10B. Quotient Register B, P/N 1159-4730.

Figure 6-10C. Readout, P/N 1159-2771.

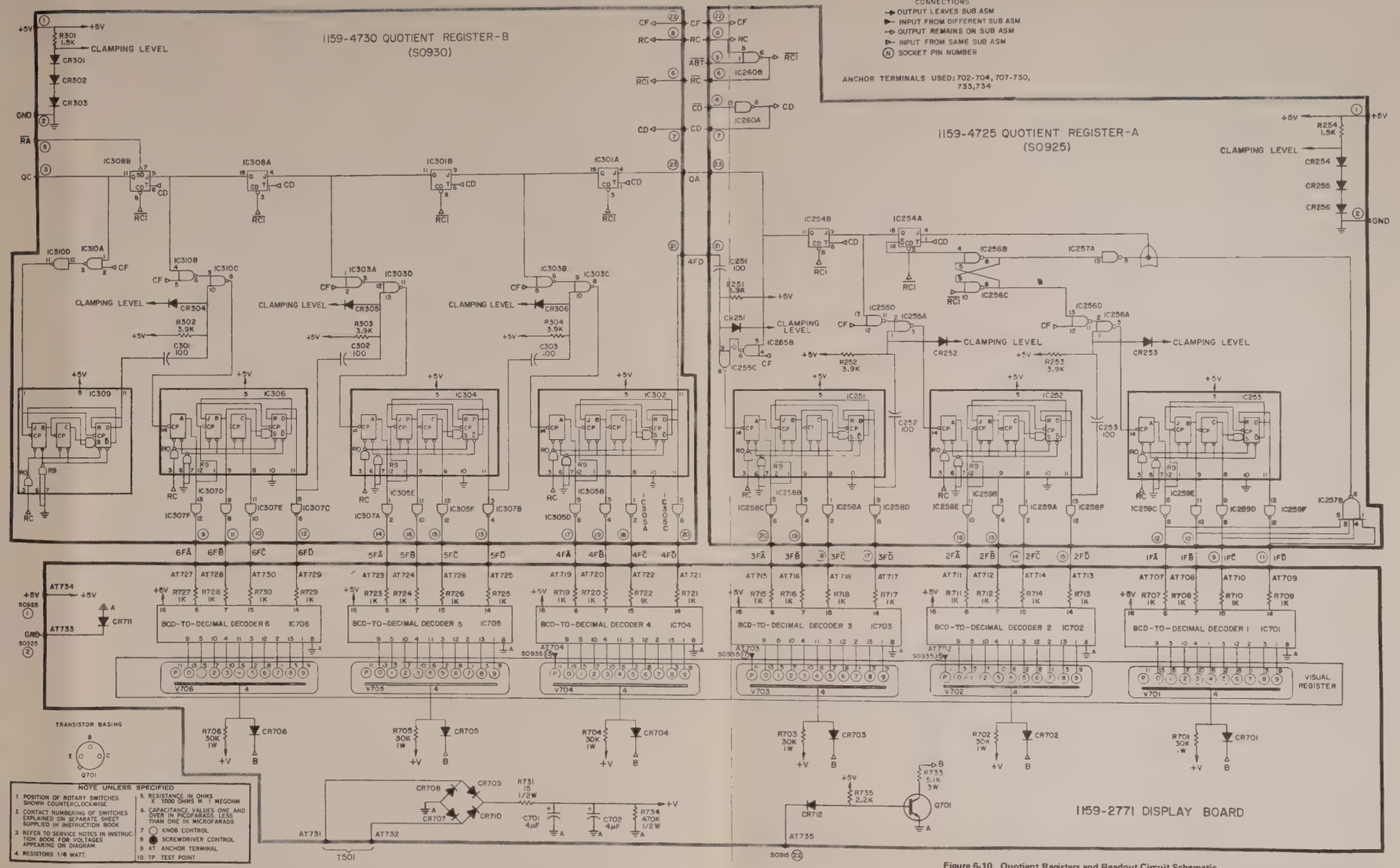

1159-4730 QUOTIENT REGISTER-B
(S0930)
1159-4725 QUOTIENT REGISTER-A
(S0925)
CONNECTIONS
OUTPUT LEAVES SUB ASM
INPUT FROM DIFFERENT SUB ASM
OUTPUT REMAINS ON SUB ASM
INPUT FROM SAME SUB ASM
(N) SOCKET PIN NUMBER
ANCHOR TERMINALS USED: 702-704, 707-730, 733,734
CLAMPING LEVEL
BCD-TO-DECIMAL DECODER 6 IC706
BCD-TO-DECIMAL DECODER 5 IC705
BCD-TO-DECIMAL DECODER 4 IC704
BCD-TO-DECIMAL DECODER 3 IC703
BCD-TO-DECIMAL DECODER 2 IC702
BCD-TO-DECIMAL DECODER 1 IC701
VISUAL REGISTER
TRANSISTOR BASING
NOTE UNLESS SPECIFIED
1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM
4. RESISTORS 1/4 WATT.
5. RESISTANCE IN OHMS K 1000 OHMS M 1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN MICROFARADS. LESS THAN ONE IN MICROFARADS
7. KNOB CONTROL
8. SCREWDRIVER CONTROL
9. AT ANCHOR TERMINAL
10. TP TEST POINT
1159-2771 DISPLAY BOARD

Figure 6-10. Quotient Registers and Readout Circuit Schematic.

6-27/28

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C451	Ceramic, 100 pF ±10% 500 V	4404-1108	72982	831, 100 pF ±10%	
C452	Ceramic, 0.01 µF +80-20% 500 V	4401-3100	80131	CC61, 0.01 µF +80-20%	5910-974-5697
C453	Ceramic, 0.05 µF +80-20% 500 V	4403-3500	01121	40-503W	5910-883-7321
DIODES					
CR451 thru CR454	Type 1N4009	6082-1012	24446	1N4009	
INTEGRATED CIRCUITS					
IC451		5431-9462	072e3	DTµL-946	
IC452		5431-8172	01295	SN7472N	
IC453		5431-8100	01295	SN7400N	
IC454		5431-8172	01295	SN7472N	
IC455		5431-8100	01295	SN7400N	
IC456		5431-8172	01295	SN7472N	
IC457		5431-8140	01295	SN7440N	
IC458		5431-8176	01295	SN7476N	
IC459		5431-8211	01295	SN74H11N	
IC460		5431-8176	01295	SN7476N	
IC461		5431-8253	01295	SN74H53N	
RESISTORS					
R451	Composition, 2.2 kΩ ±10% 1/4 W	6099-2229	75042	BTS, 2.2 kΩ ±10%	
R452	Composition, 180Ω ±5% 1/4 W	6099-1185	75042	BTS, 180 Ω ±5%	5905-279-5476
R457	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R458 thru R459	Composition, 6.8 kΩ ±10% 1/4 W	6099-2689	75042	BTS, 6.8 kΩ ±10%	
R460	Composition, 10 kΩ ±10% 1/4 W	6099-3109	75042	BTS, 10 kΩ ±10%	
R461	Composition, 8.2 kΩ ±10% 1/4 W	6099-2829	75042	BTS, 8.2 kΩ ±10%	

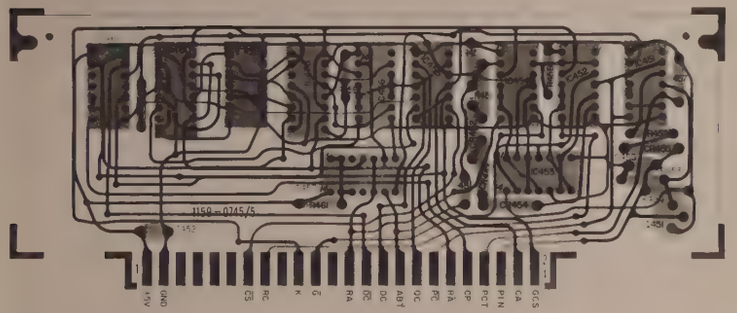


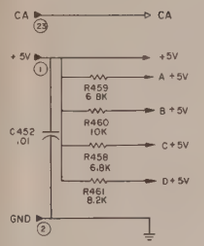
Figure 6-11. Add Cycle and Reset, P/N 1159-4745.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

NOTE UNLESS SPECIFIED

1. POSITION OF ROTARY SWITCHES SHOWN COUNTERCLOCKWISE
2. CONTACT NUMBERING OF SWITCHES EXPLAINED ON SEPARATE SHEET SUPPLIED IN INSTRUCTION BOOK
3. REFER TO SERVICE NOTES IN INSTRUCTION BOOK FOR VOLTAGES APPEARING ON DIAGRAM
4. RESISTORS 1/4 WATT
5. RESISTANCE IN OHMS K - 1000 OHMS M - 1 MEGOHM
6. CAPACITANCE VALUES ONE AND OVER IN PICOFARADS, LESS THAN ONE IN MICROFARADS
7. ○ KNOB CONTROL
8. ● SCREWDRIVER CONTROL
9. AT - ANCHOR TERMINAL
10. TP - TEST POINT

→ OUTPUT LEAVES SUBASSEMBLY
▶ INPUT FROM DIFFERENT SUBASSEMBLY
→ OUTPUT REMAINS ON SUBASSEMBLY
▷ INPUT FROM SAME SUBASSEMBLY
(N) SOCKET PIN NUMBER



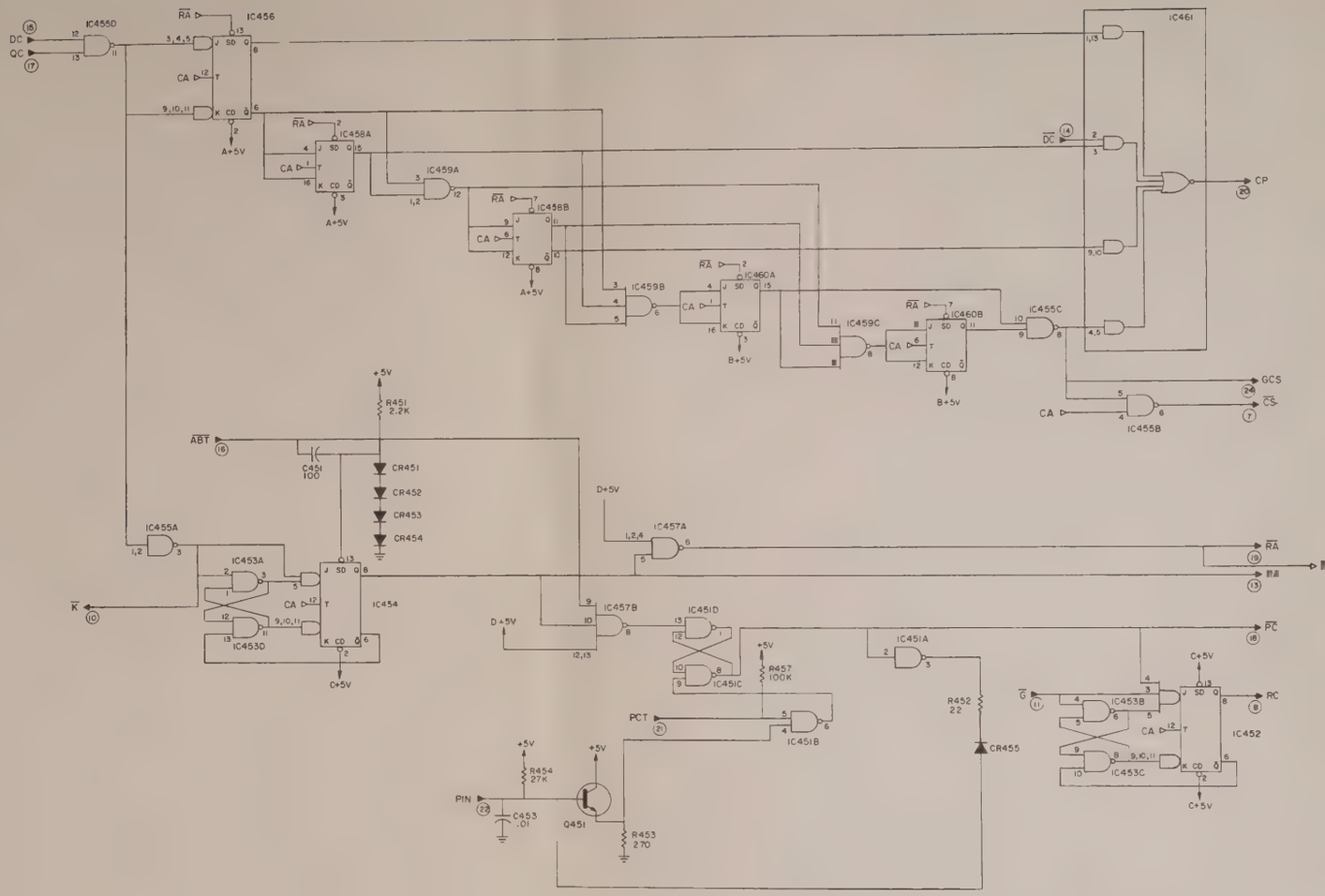


Figure 6-11. Add Cycle and Reset Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
CAPACITORS					
C351	Ceramic, 220 pF ±5% 500 V	4404-1225	72982	831, 220 pF ±5%	
C352	Electrolytic, 330 µF ±20% 6 V	4450-5707	37942	TT, 330 µF ±20%	
DIODES					
CR351 thru CR352	Type 1N995	6082-1002	80368	1N995	
CR353 thru CR359	Type 1N4009	6082-1012	24446	1N4009	
CR360	Type 1N995	6082-1002	80368	1N995	
CR361	Type 1N645/T156	6082-1016	24446	1N645	5961-944-8222
CR362	Type 1N995	6082-1002	80368	1N995	
INTEGRATED CIRCUITS					
IC351		5431-9362	07263	DTµL 936	
IC352		5431-9462	07263	DTµL-946	
IC353		5431-9462	07263	DTµL-946	
IC354		5431-9362	07263	DTµL-936	
IC355		5431-9462	07263	DTµL-946	
IC356		5431-8176	01295	SN7476N	
IC357		5431-8176	01295	SN7476N	
IC358		5431-9462	07263	DTµL-946	
IC359		5431-9362	07263	DTµL-936	
IC360		5431-9462	07263	DTµL-946	
RESISTORS					
R351 thru R352	Composition, 100 kΩ ±10% 1/4 W	6099-4109	75042	BTS, 100 kΩ ±10%	
R353	Composition, 180 Ω ±10% 1/4 W	6099-1189	75042	BTS, 180 Ω ±10%	
R354	Composition, 3.3 kΩ ±10% 1/4 W	6099-2339	75042	BTS, 3.3 kΩ ±10%	
R355 thru R359	Composition, 270 Ω ±10% 1/4 W	6099-1279	75042	BTS, 270 Ω ±10%	
R360	Composition, 8.2 kΩ ±10% 1/4 W	6099-2829	75042	BTS, 8.2 kΩ ±10%	
R361	Composition, 3.9 kΩ ±10% 1/4 W	6099-2399	75042	BTS, 3.9 kΩ ±10%	
R362 thru R364	Composition, 10 MΩ ±10% 1/4 W	6099-6109	75042	BTS, 10 MΩ ±10%	
INDUCTOR					
L351	56 µH ±10%	4300-6390	99800	3500, 56 µH ±10%	
TRANSISTORS					
Q351 thru Q353	Type 2N3416	8210-1138	93916	2N3416	
Q354 thru Q358	Type 2N3416	8210-1096	07263	2N3638	
Q359	Type 2N3416	8210-1123	93916	2N4123	

Figure 6-12. Range Counter, P/N 1159-4735.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

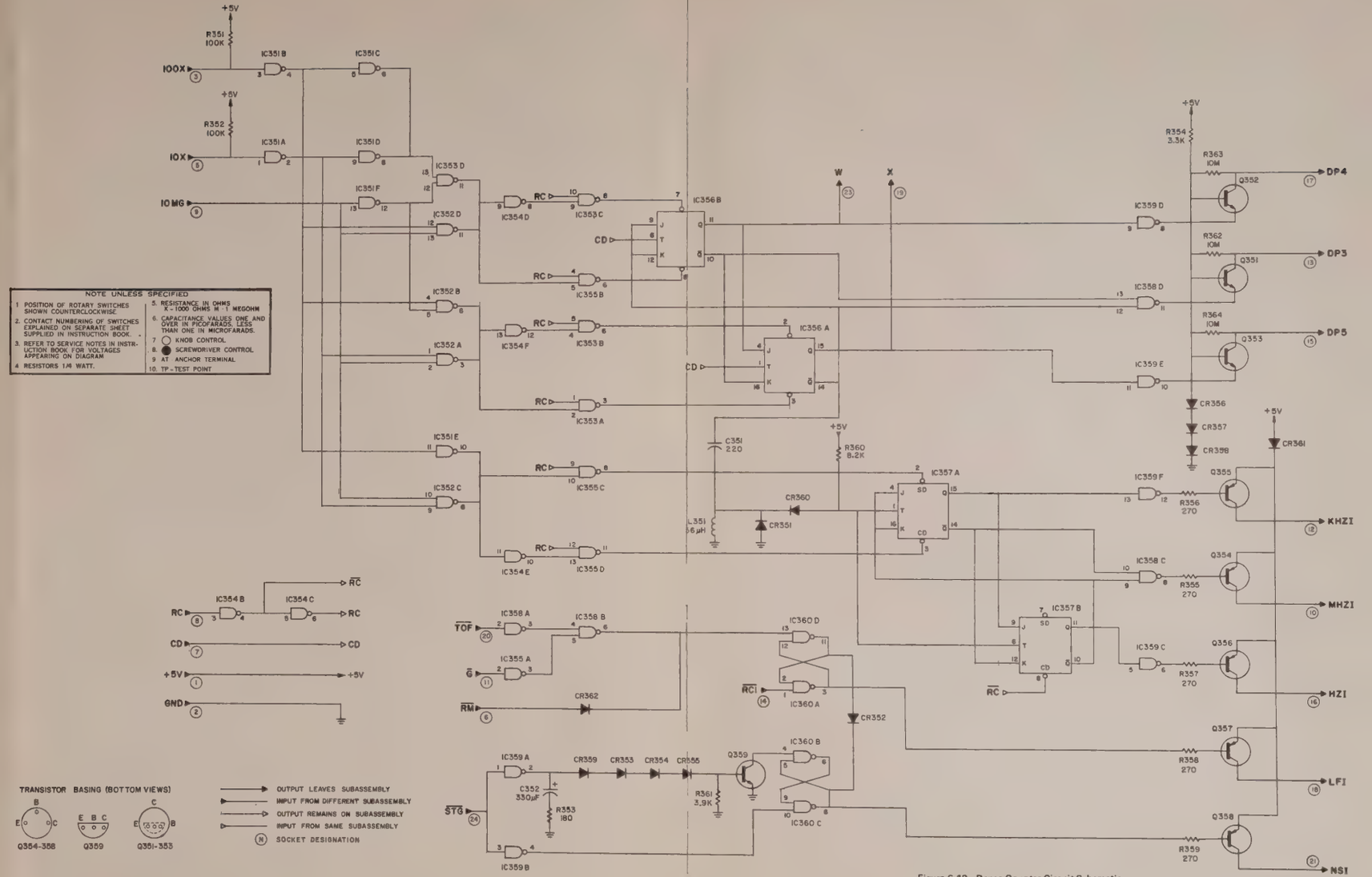


Figure 6-12. Range Counter Circuit Schematic.

Ref. No.	Description	Part No.	Fed. Mfg. Code	Mfg. Part No.	Fed. Stock No.
INTEGRATED CIRCUITS					
IC801 thru IC805	Integrated Circuit, Digital	5431-9362	07263	DTμL-936	

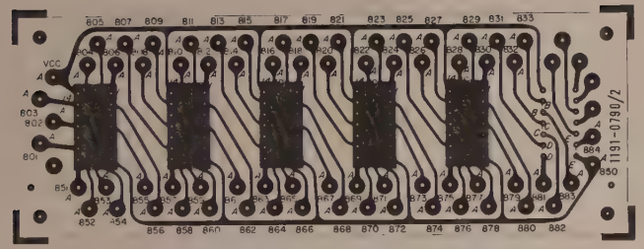


Figure 6-13. Buffer, P/N 1159-2790.

NOTE: The number appearing on the foil side is not the part number. The dot on the foil at the transistor socket indicates the collector lead.

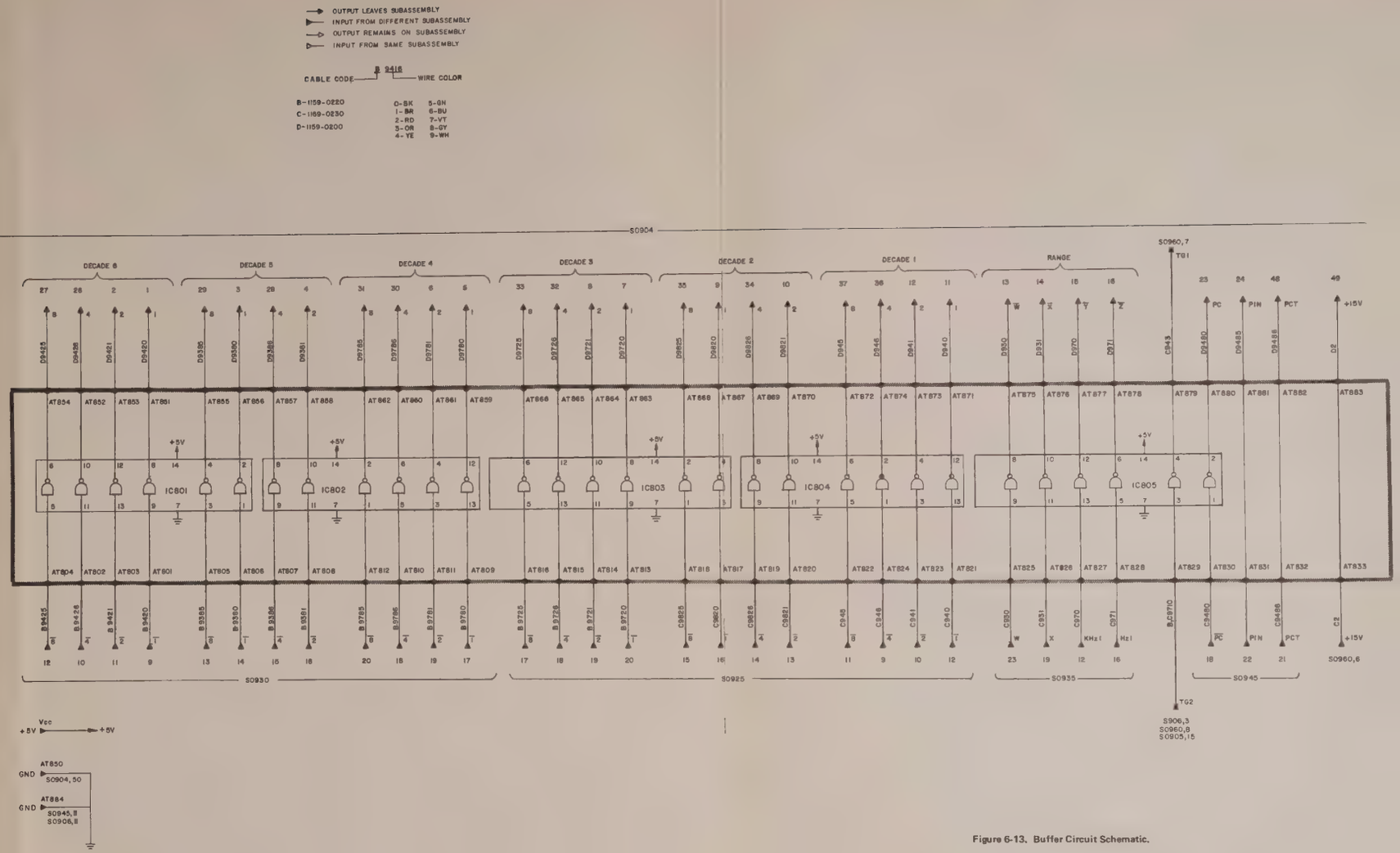


Figure 6-13. Buffer Circuit Schematic.

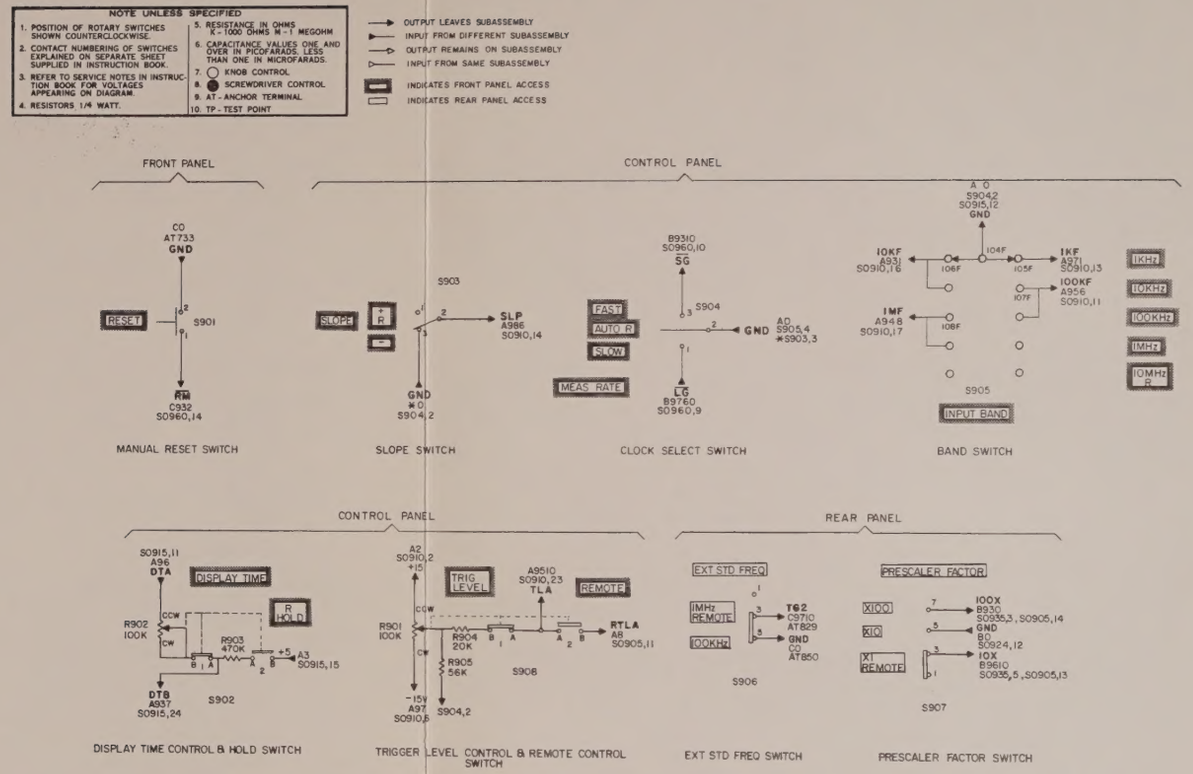


Figure 6-14. Control Wiring Diagram.

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